

TITLE: INTEGRATED CIRCUIT AND SEED LAYERS
INVENTORS NAME: Paul A. Farrar
DOCKET NO.: 303.673US3

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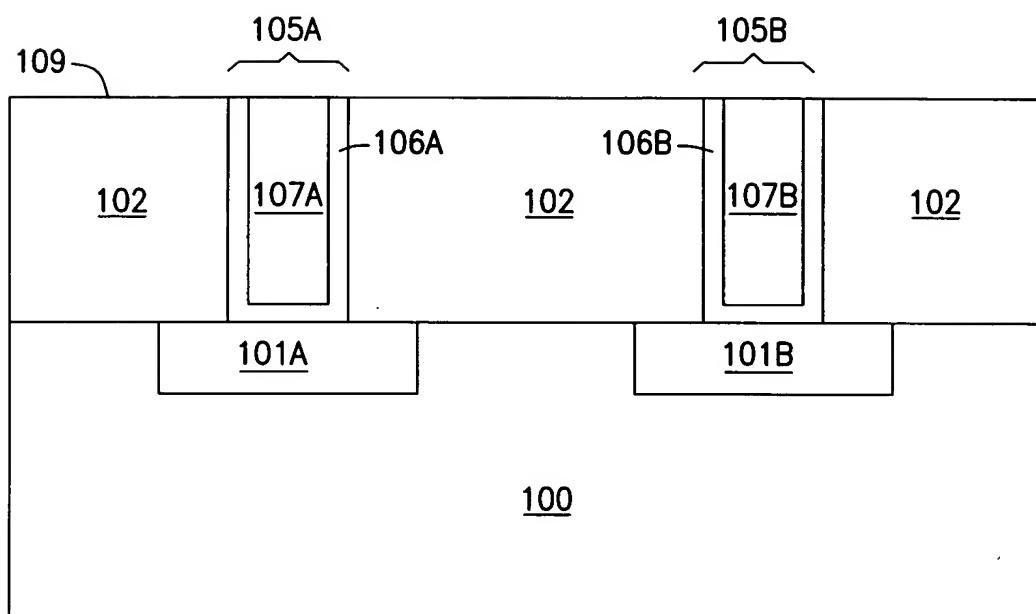


FIG. 1A

TITLE: INTEGRATED CIRCUIT AND SEED LAYERS
INVENTORS NAME: Paul A. Farrar
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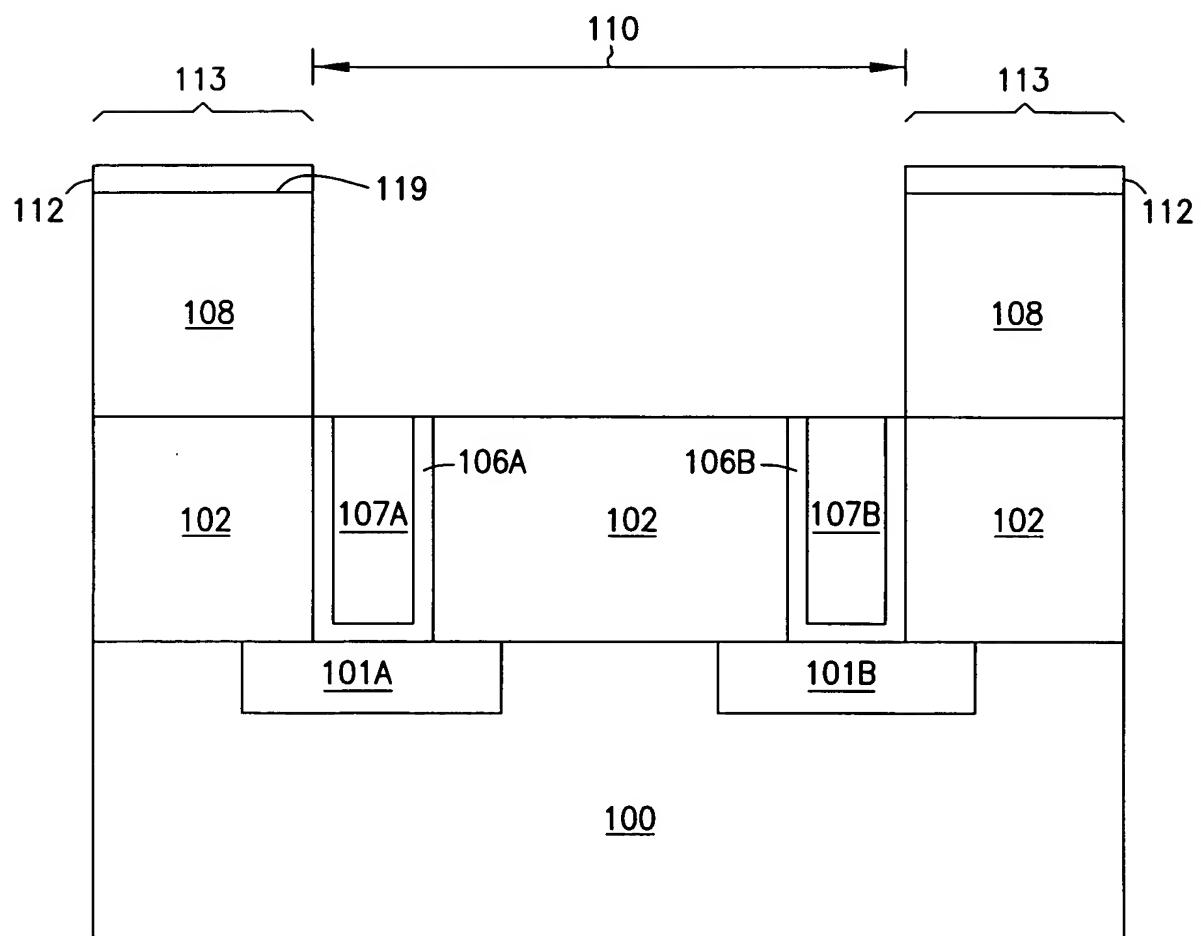


FIG. 1B

TITLE: INTEGRATED CIRCUIT AND SEED LAYERS
INVENTORS NAME: Paul A. Farrar
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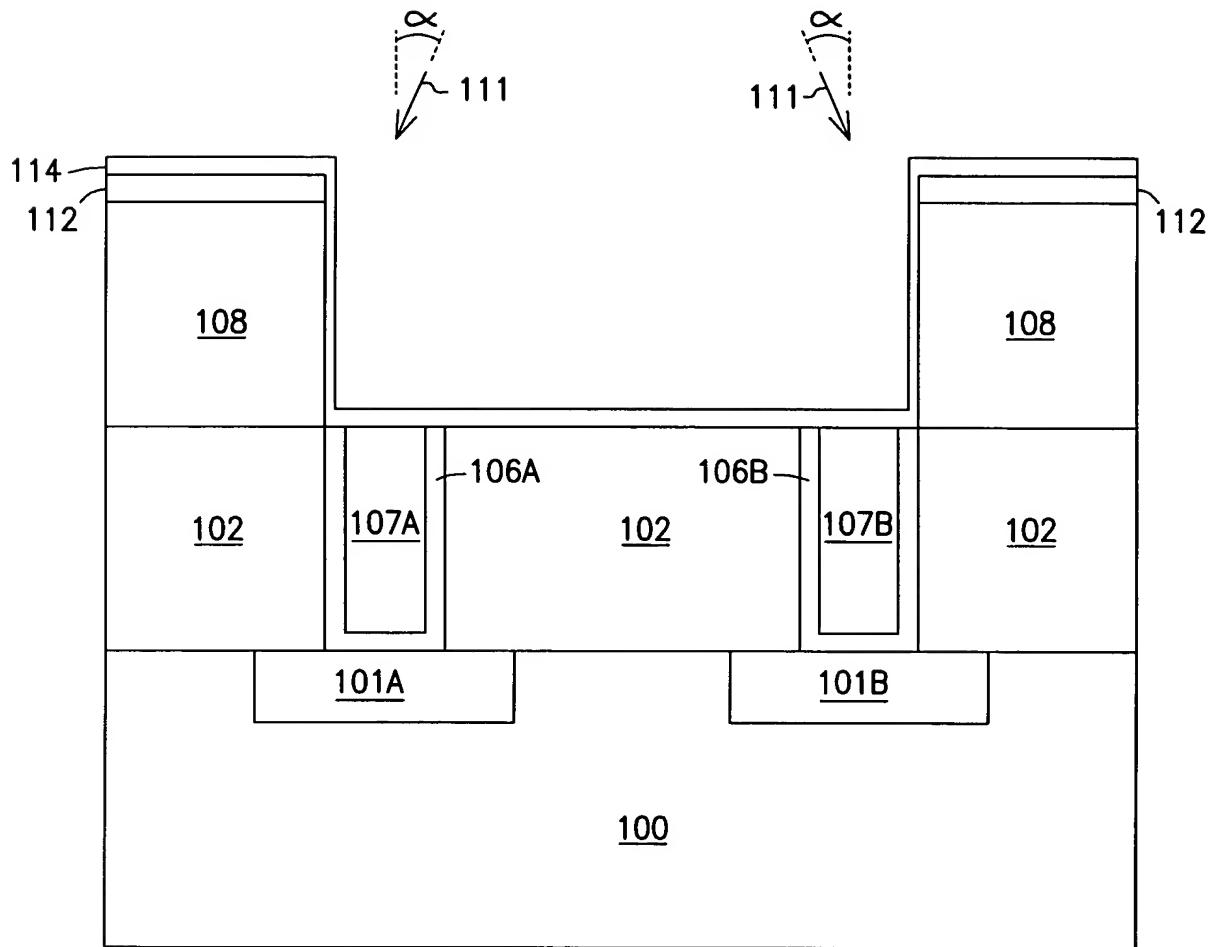


FIG. 1C

TITLE: INTEGRATED CIRCUIT AND SEED LAYERS

INVENTORS NAME: Paul A. Farrar

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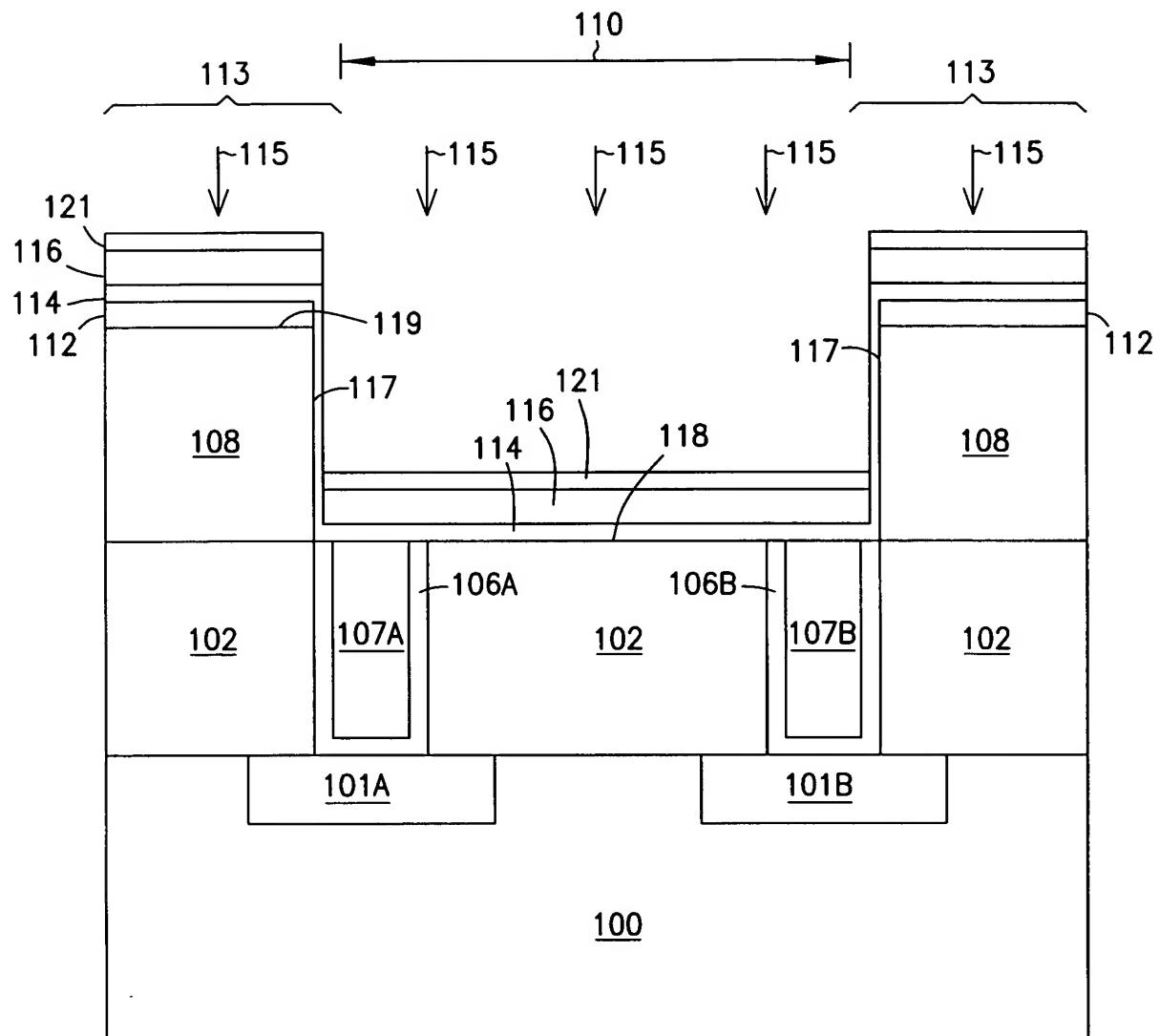


FIG. 1D

TITLE: INTEGRATED CIRCUIT AND SEED LAYERS
INVENTORS NAME: Paul A. Farrar
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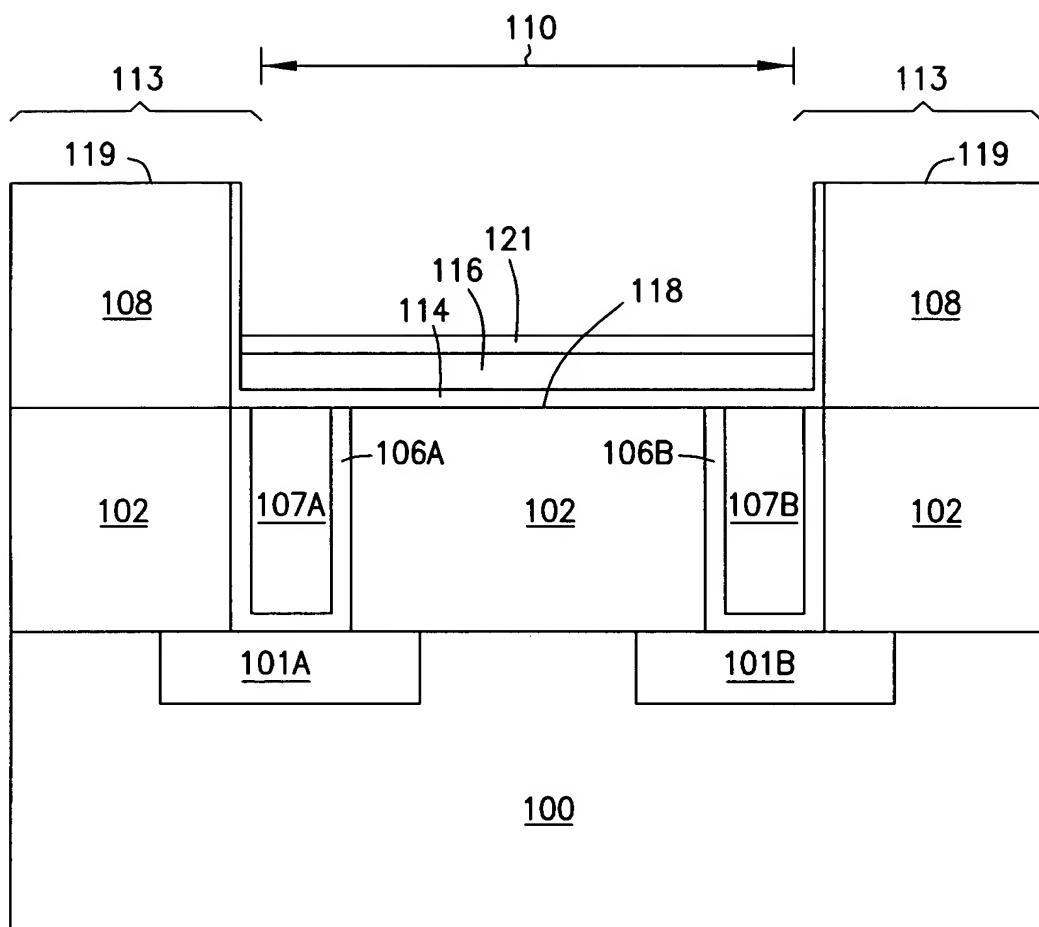


FIG. 1E

TITLE: INTEGRATED CIRCUIT AND SEED LAYERS
INVENTORS NAME: Paul A. Farrar
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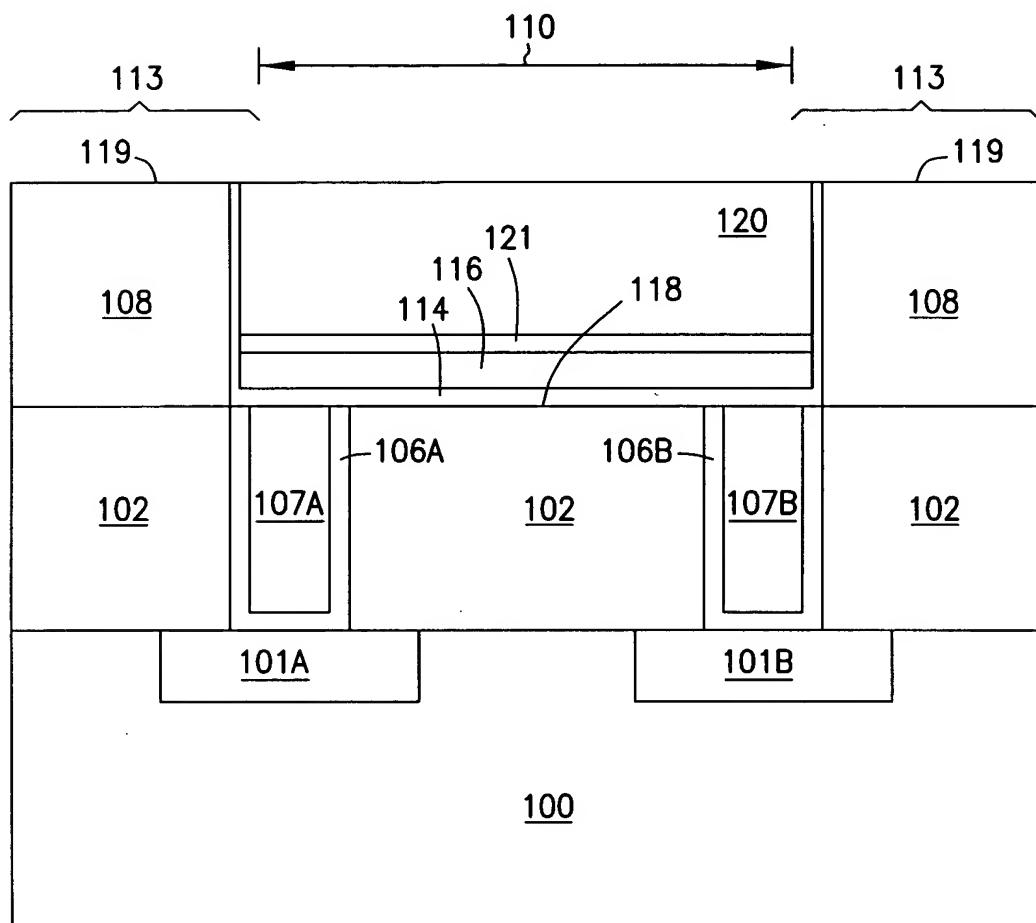


FIG. 1F

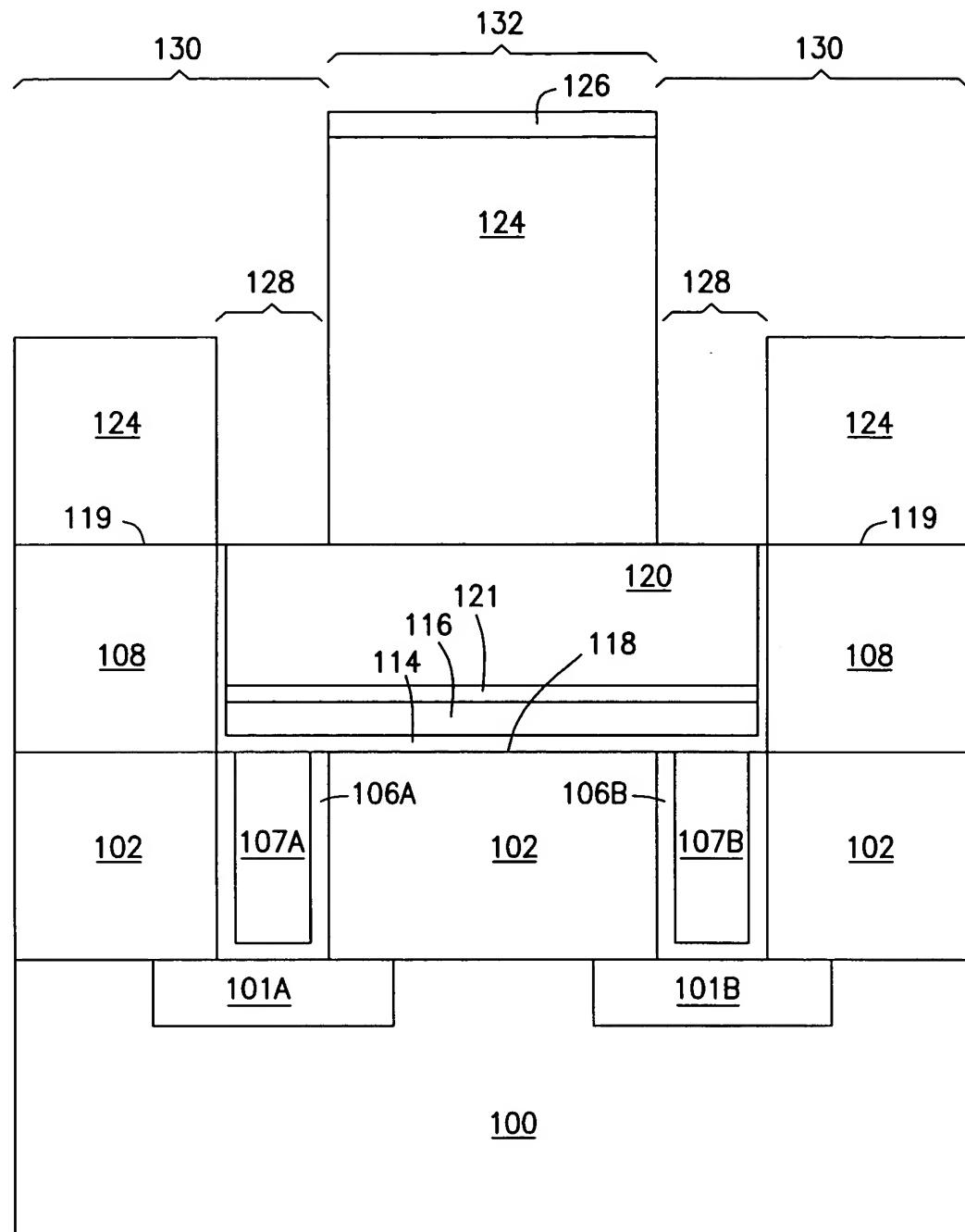


FIG. 1G

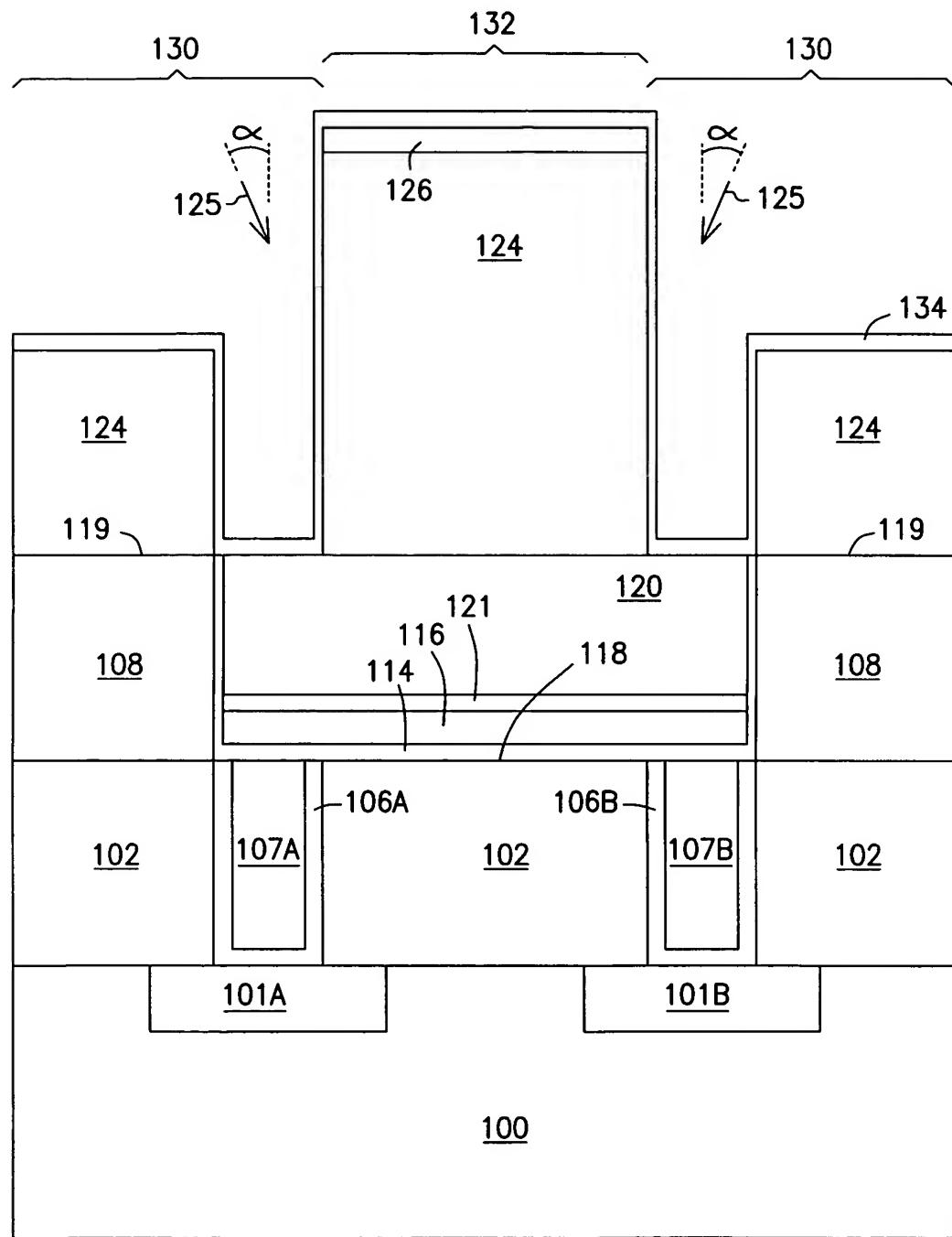


FIG. 1H

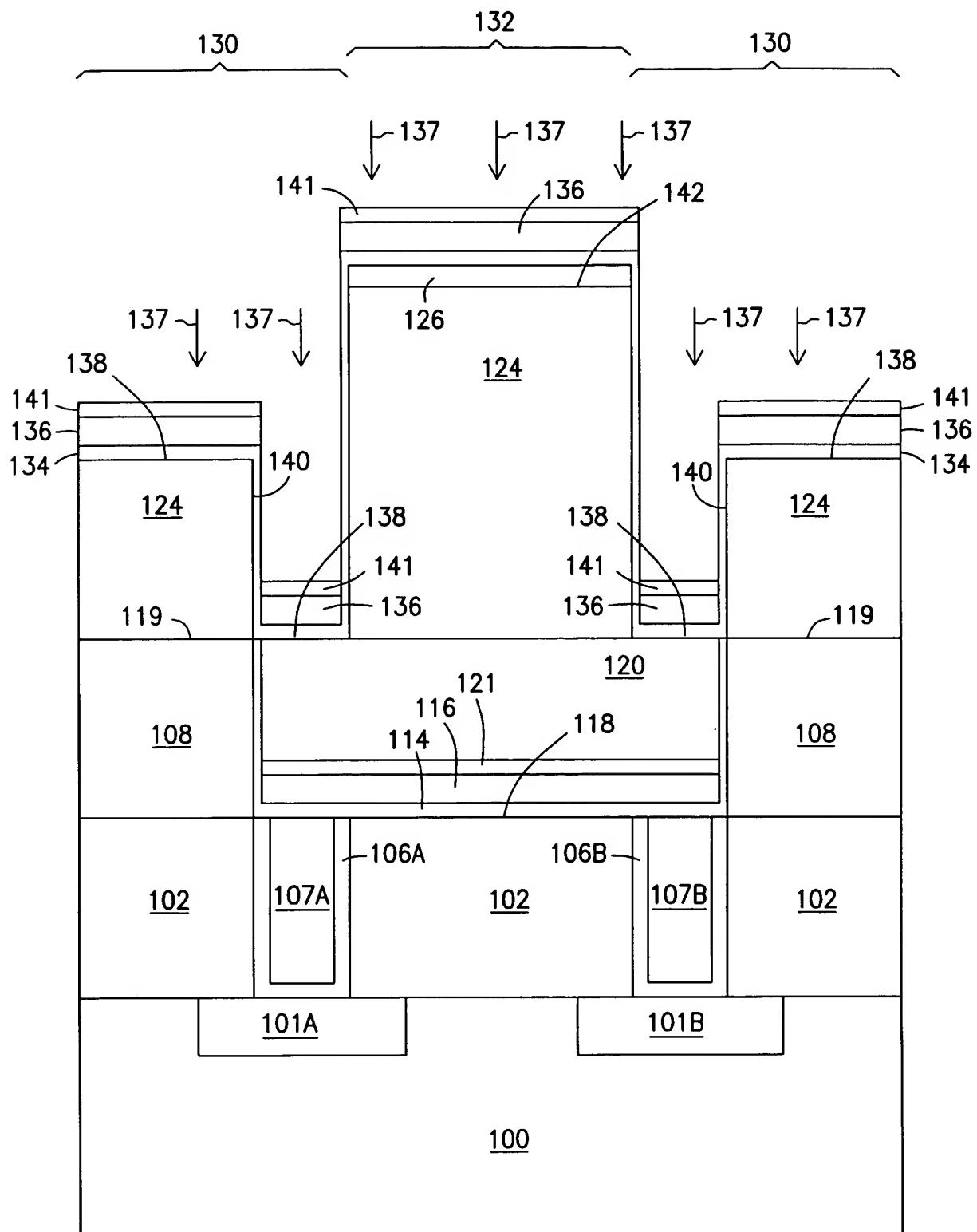


FIG. 11

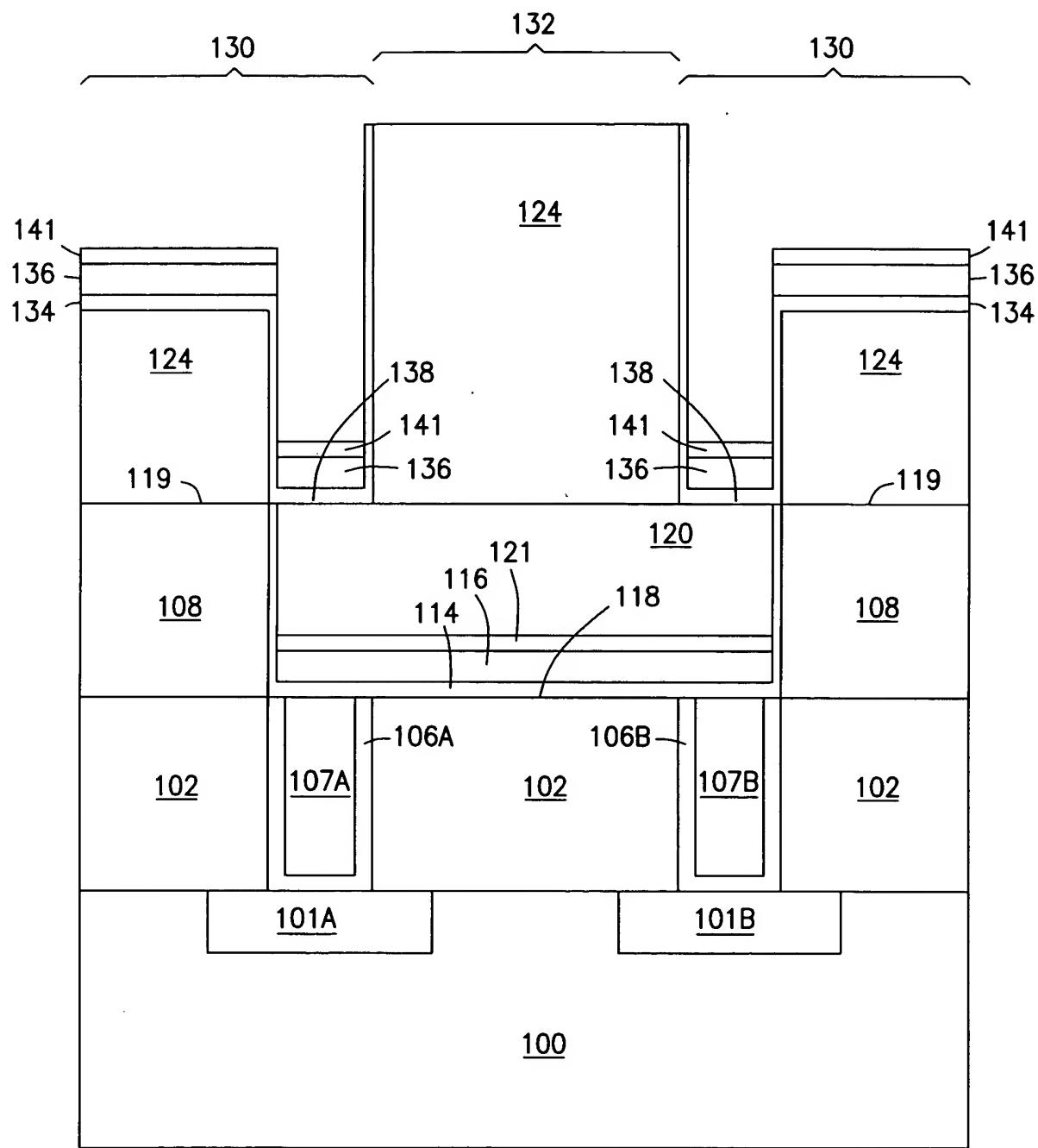


FIG. 1J

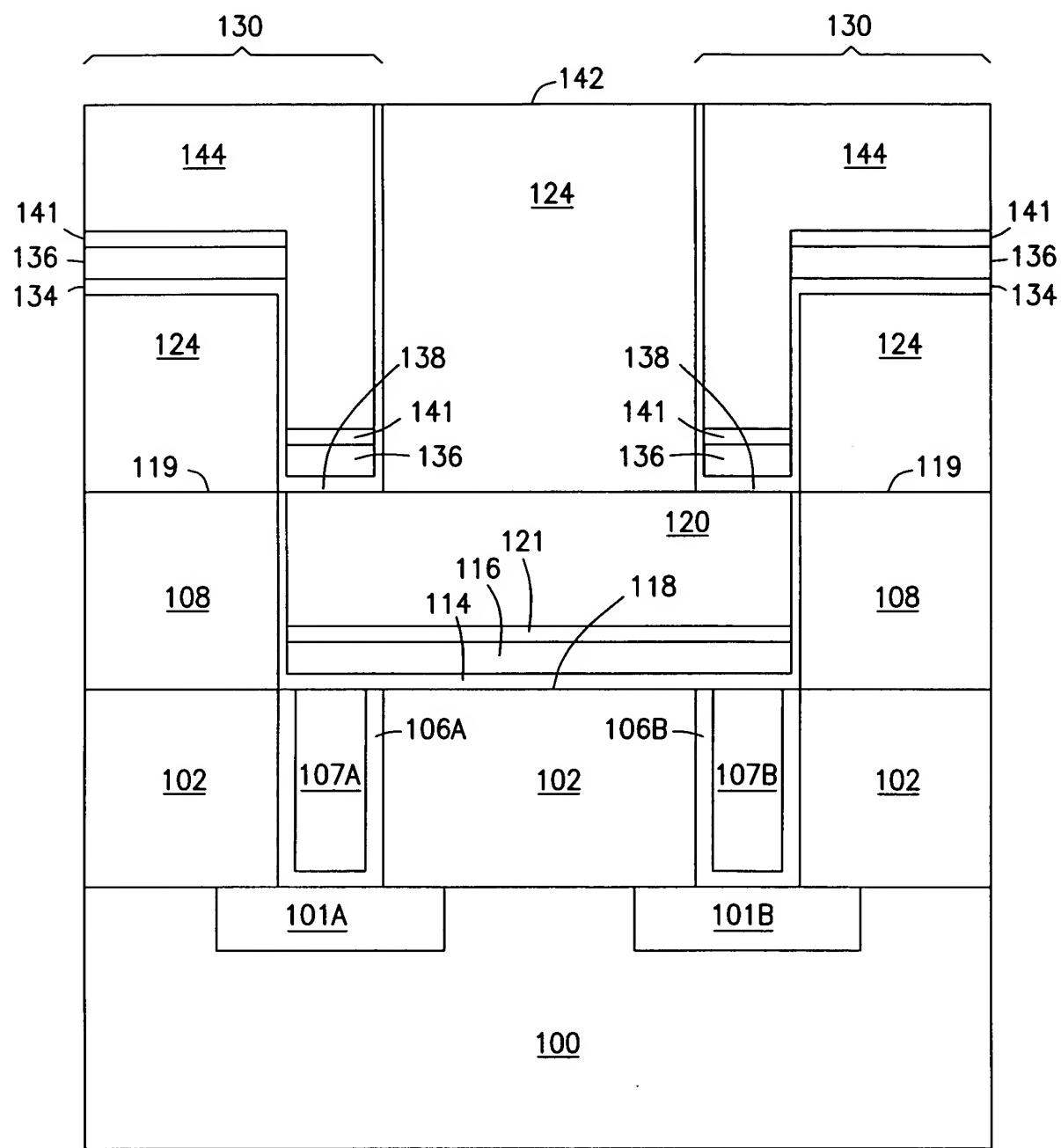


FIG. 1K

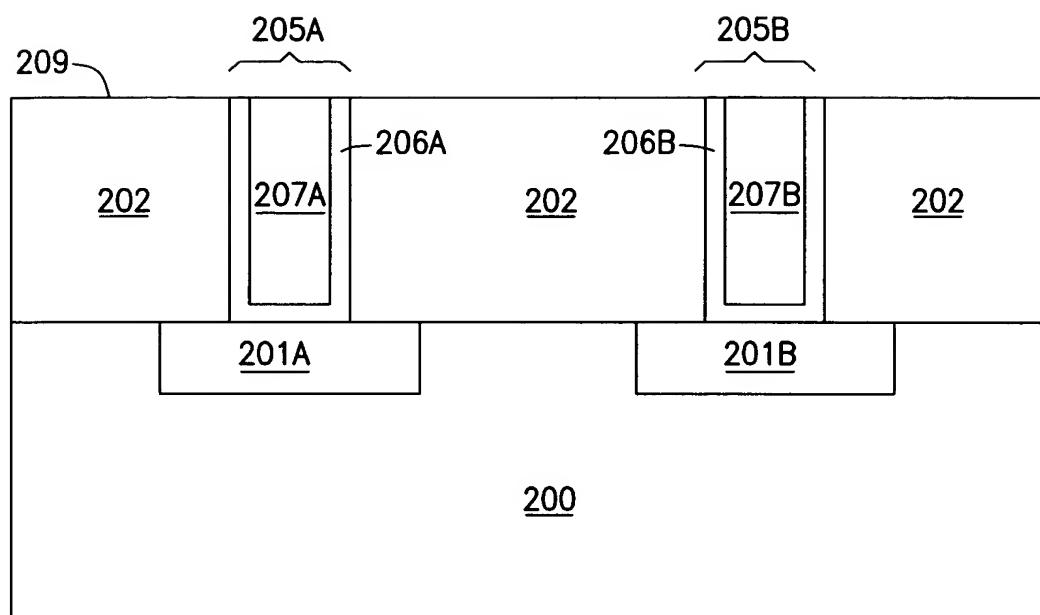


FIG. 2A

TITLE: INTEGRATED CIRCUIT AND SEED LAYERS
INVENTORS NAME: Paul A. Farrar
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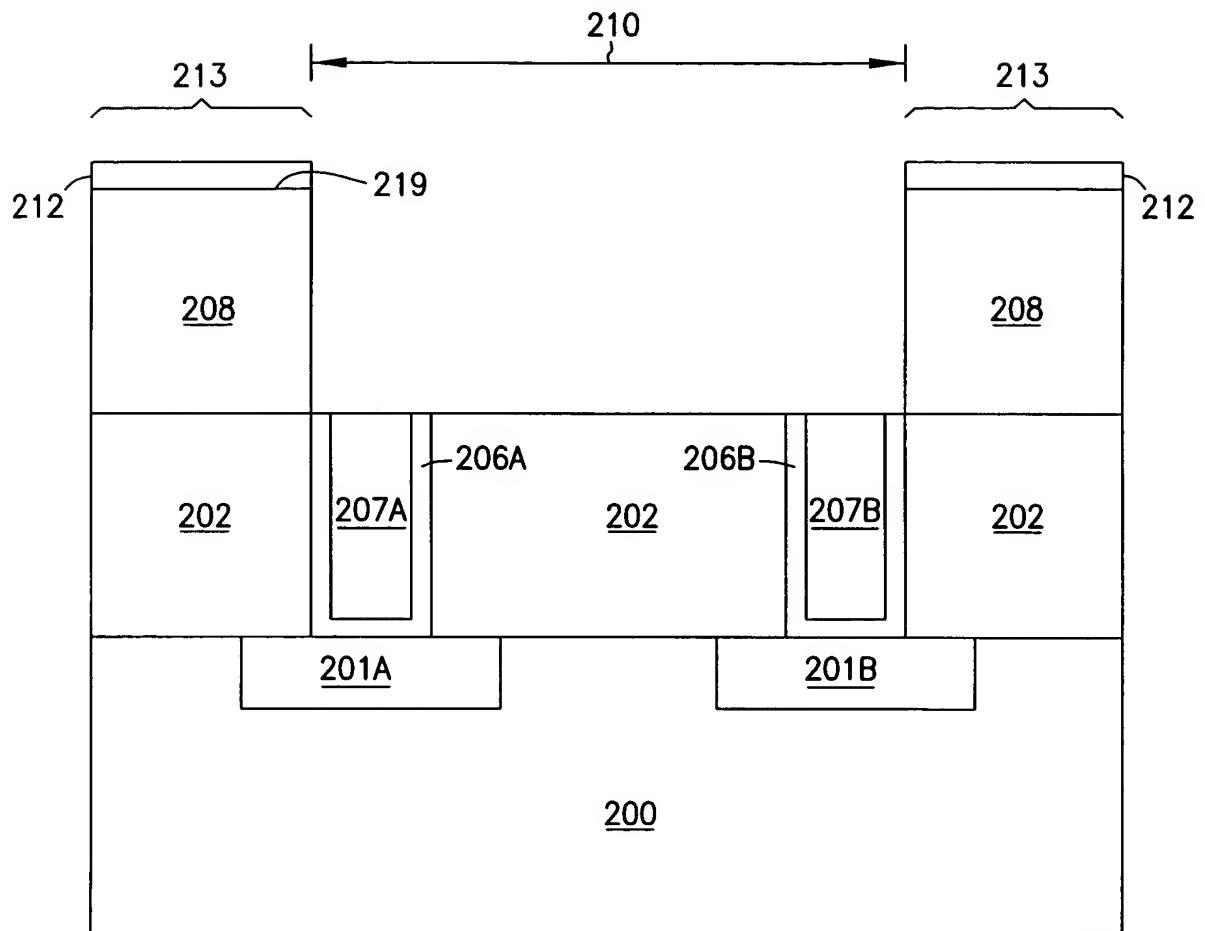


FIG. 2B

TITLE: INTEGRATED CIRCUIT AND SEED LAYERS

INVENTORS NAME: Paul A. Farrar

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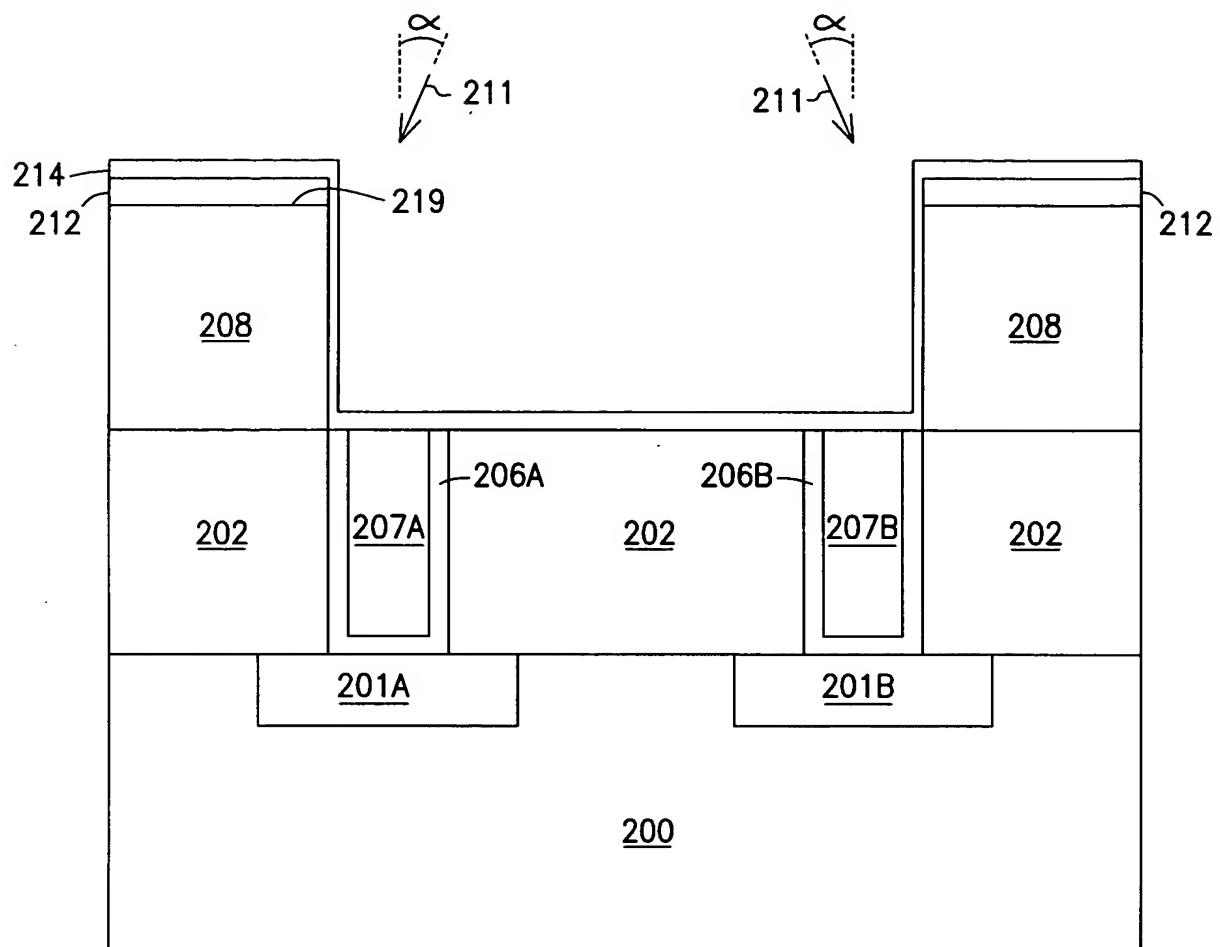


FIG. 2C

TITLE: INTEGRATED CIRCUIT AND SEED LAYERS

INVENTORS NAME: Paul A. Farrar

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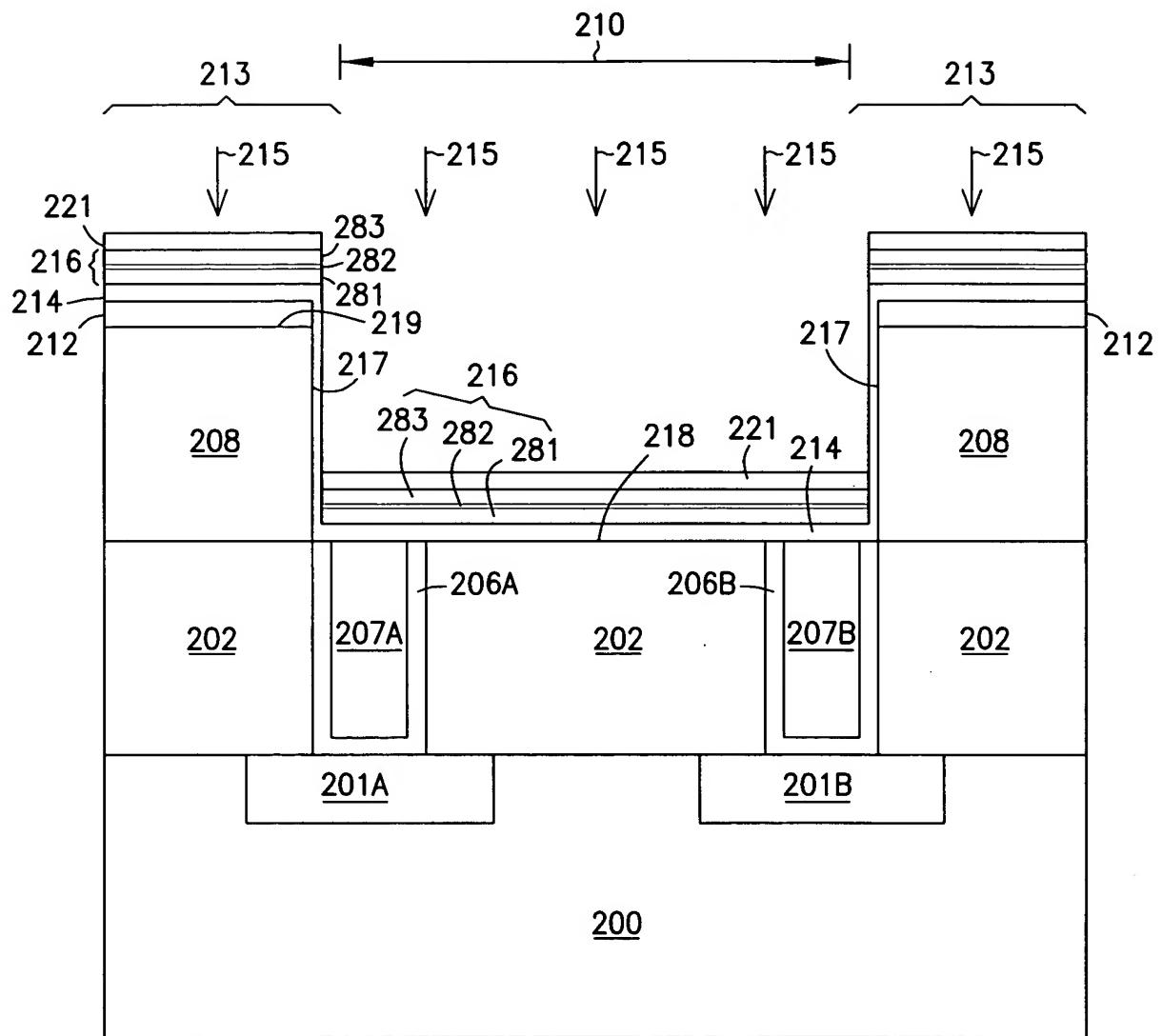


FIG. 2D

TITLE: INTEGRATED CIRCUIT AND SEED LAYERS

INVENTORS NAME: Paul A. Farrar

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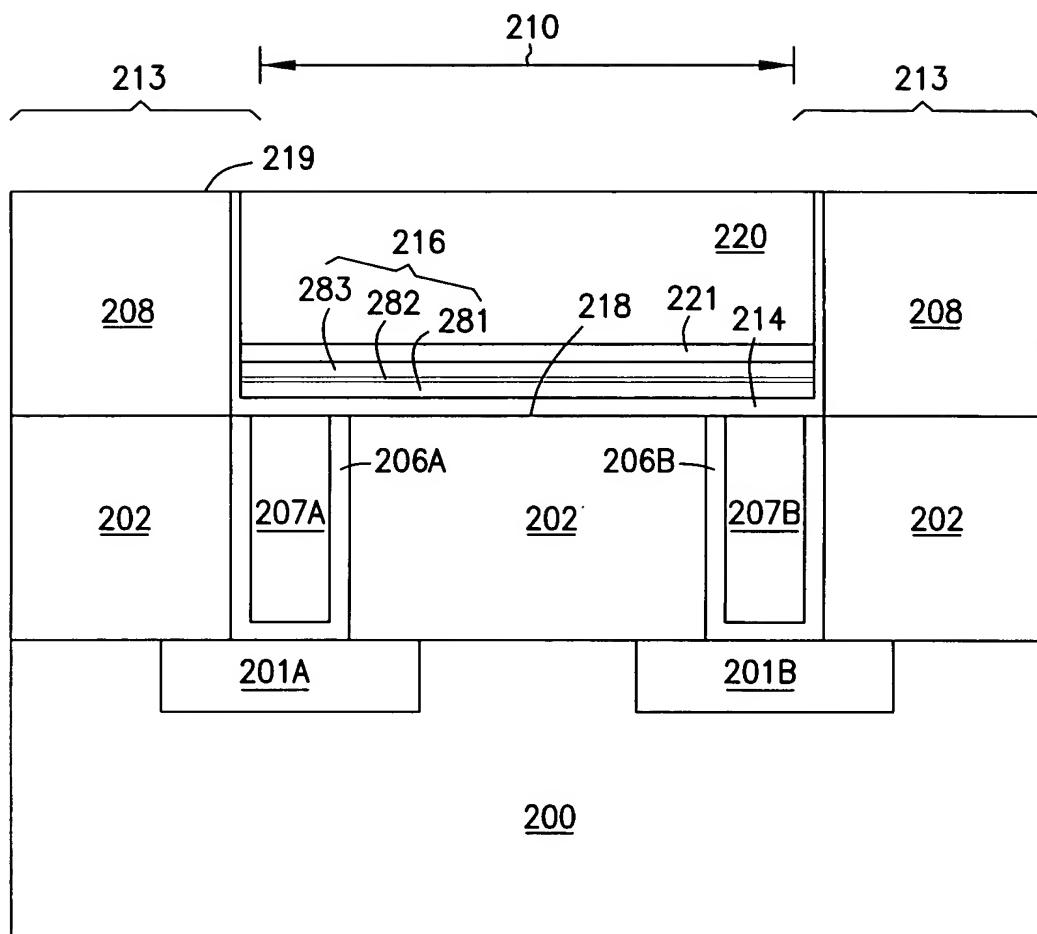


FIG. 2E

TITLE: INTEGRATED CIRCUIT AND SEED LAYERS
INVENTORS NAME: Paul A. Farrar
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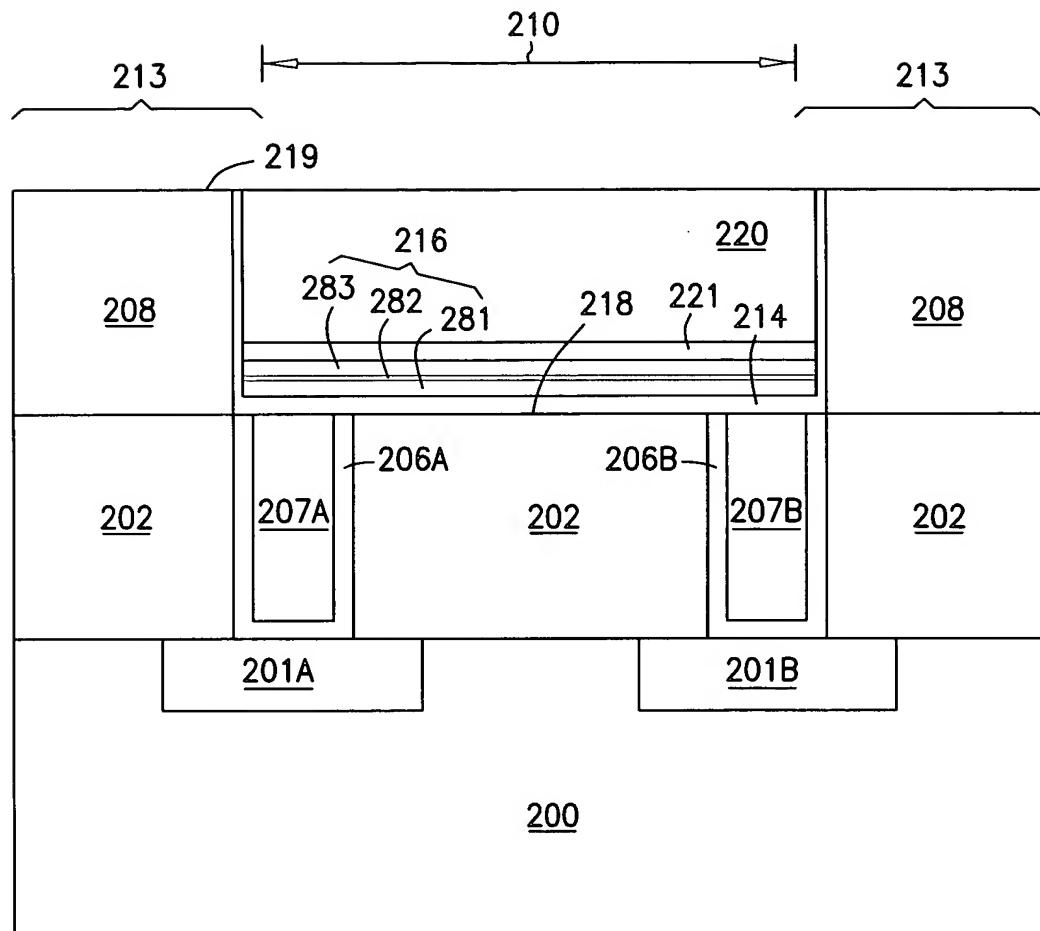


FIG. 2F

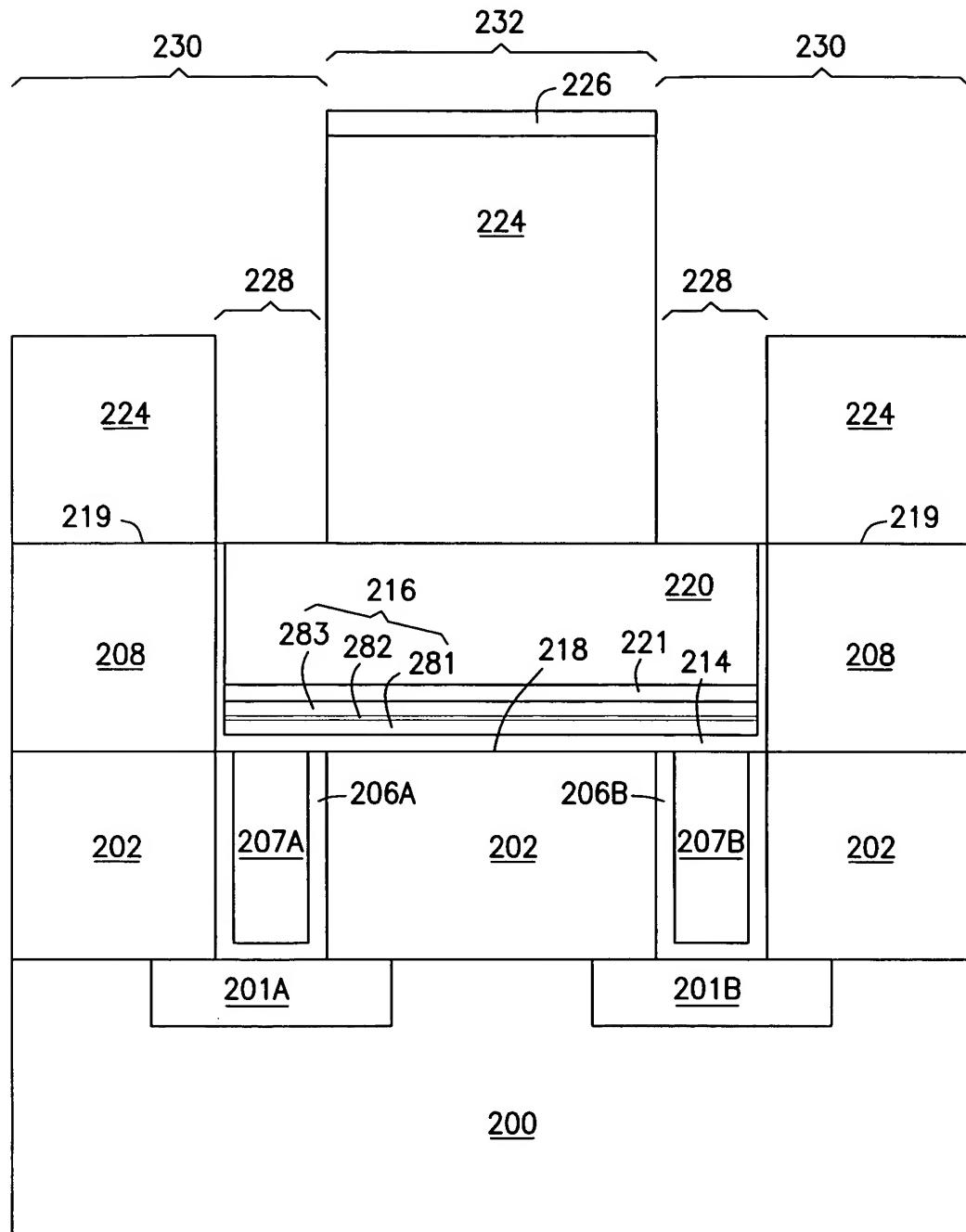


FIG. 2G

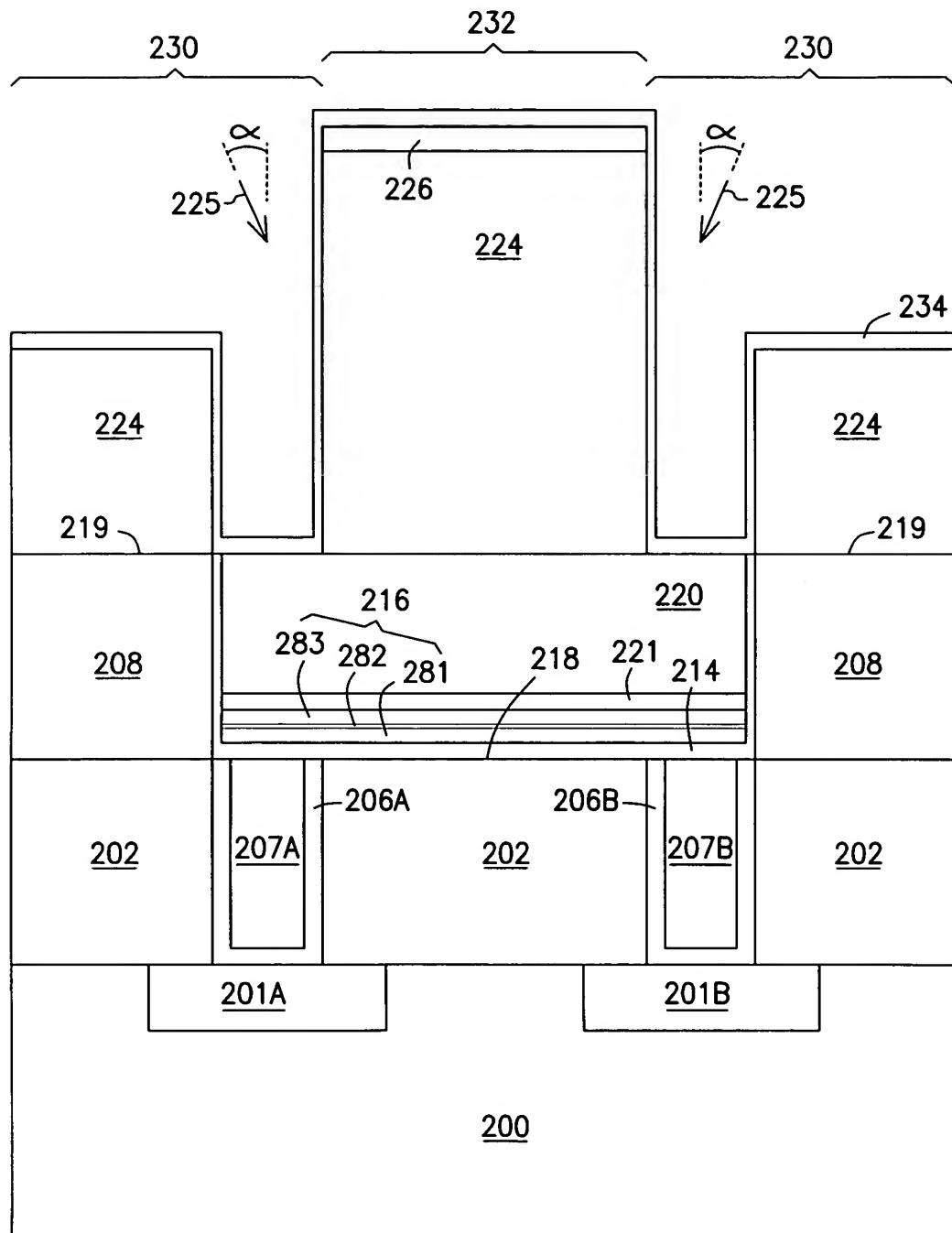


FIG. 2H

TITLE: INTEGRATED CIRCUIT AND SEED LAYERS

INVENTORS NAME: Paul A. Farrar

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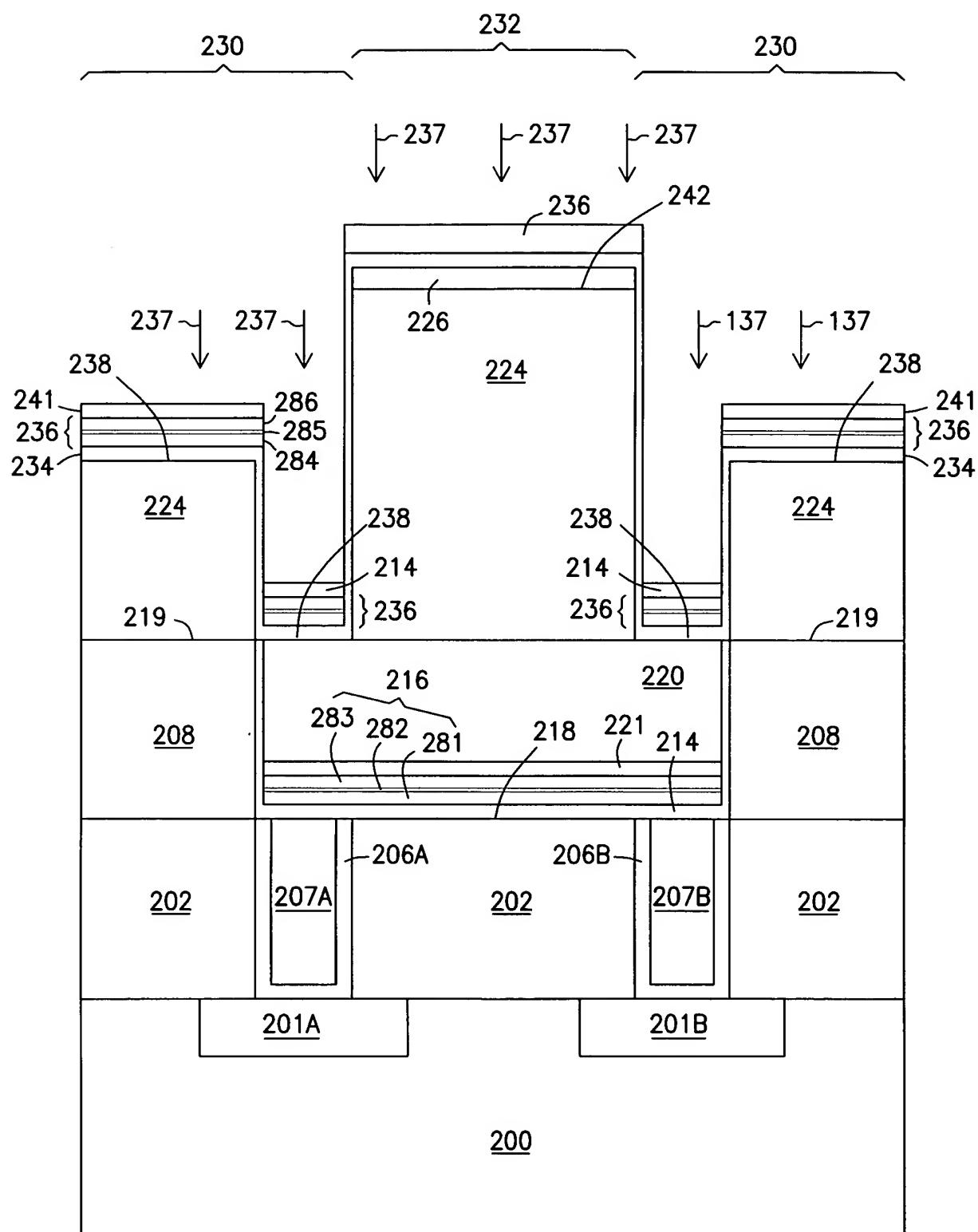


FIG. 2I

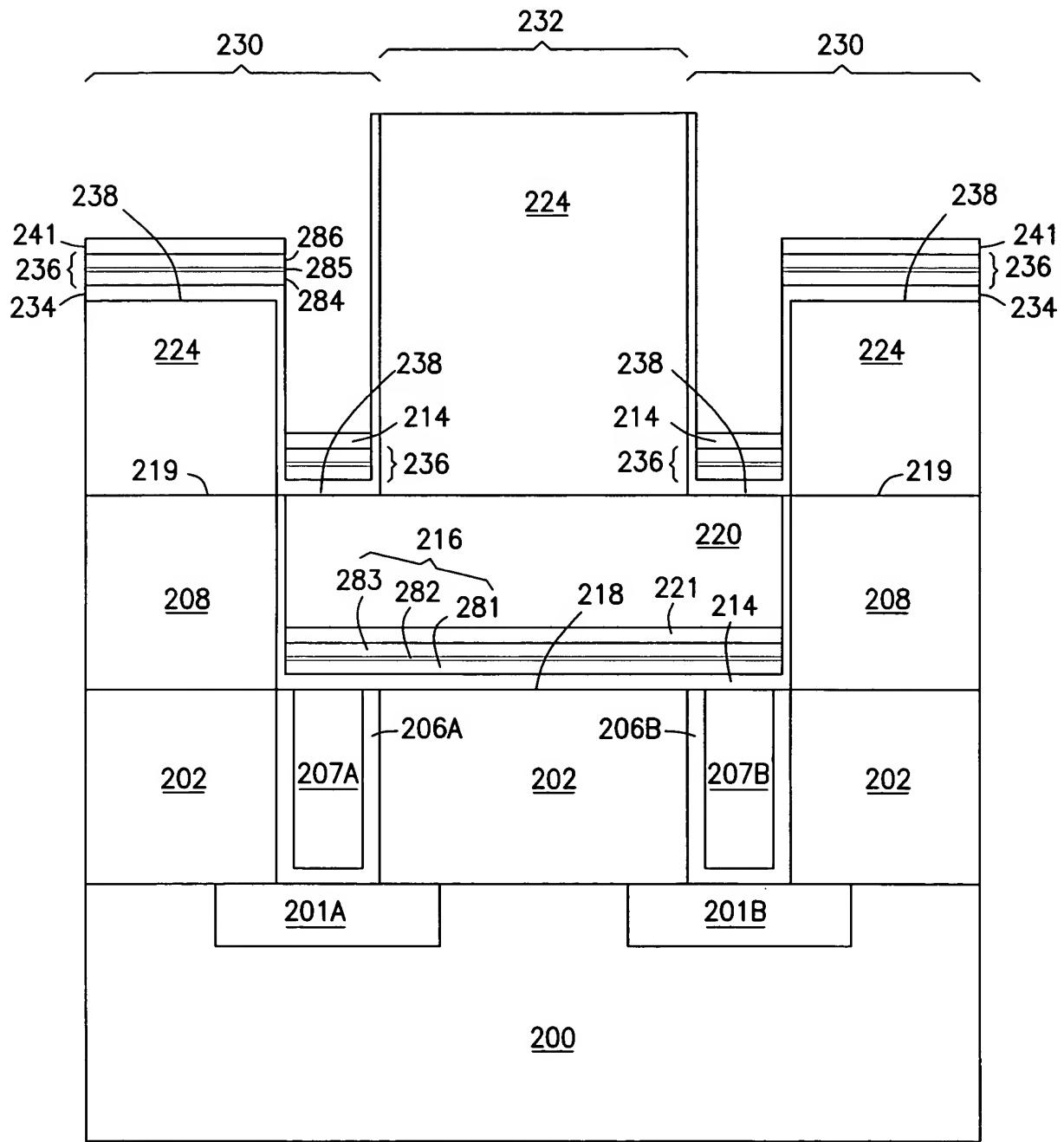


FIG. 2J

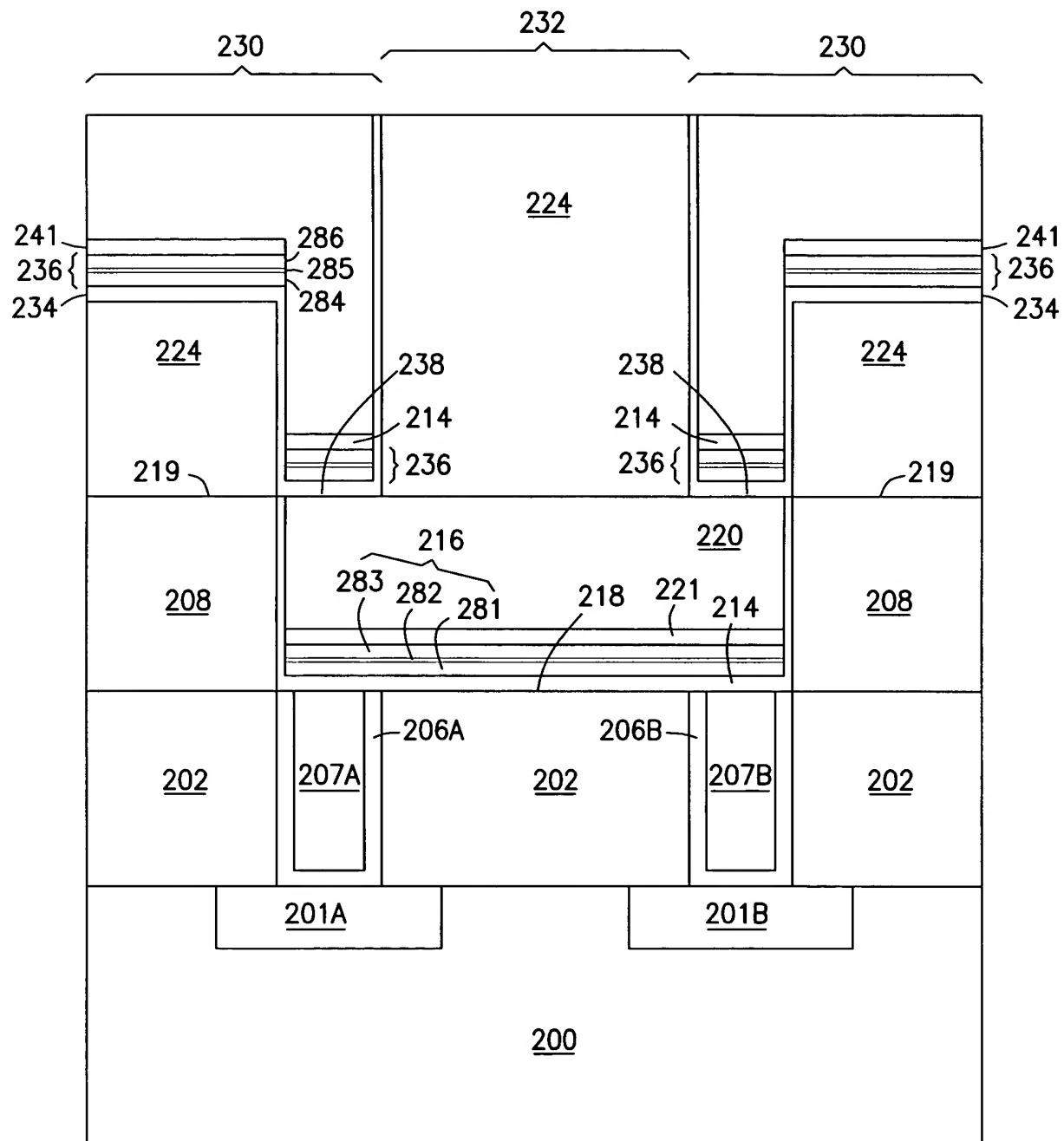


FIG. 2K

TITLE: INTEGRATED CIRCUIT AND SEED LAYERS
INVENTORS NAME: Paul A. Farrar
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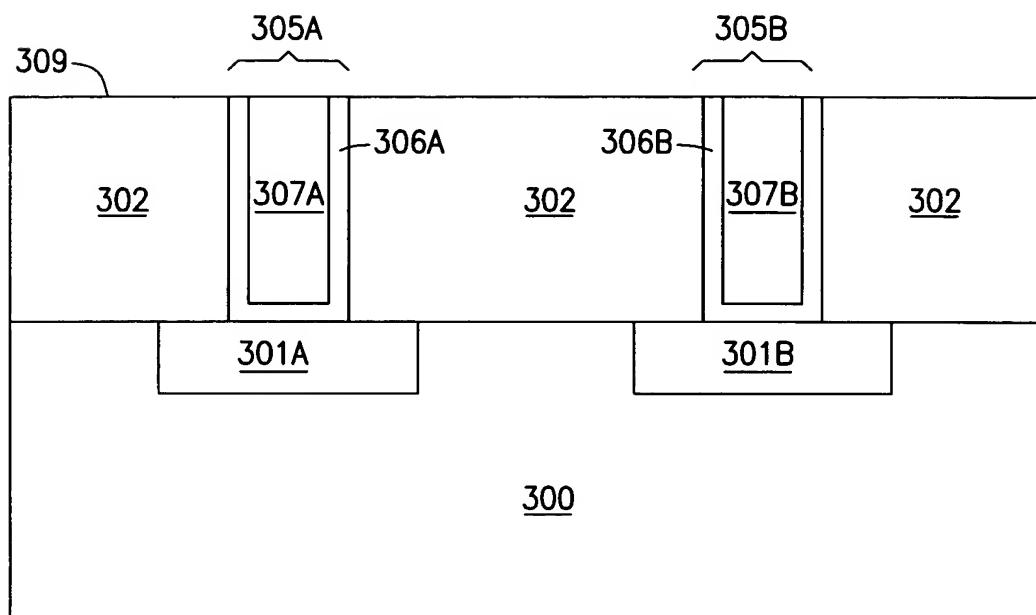


FIG. 3A

TITLE: INTEGRATED CIRCUIT AND SEED LAYERS
INVENTORS NAME: Paul A. Farrar
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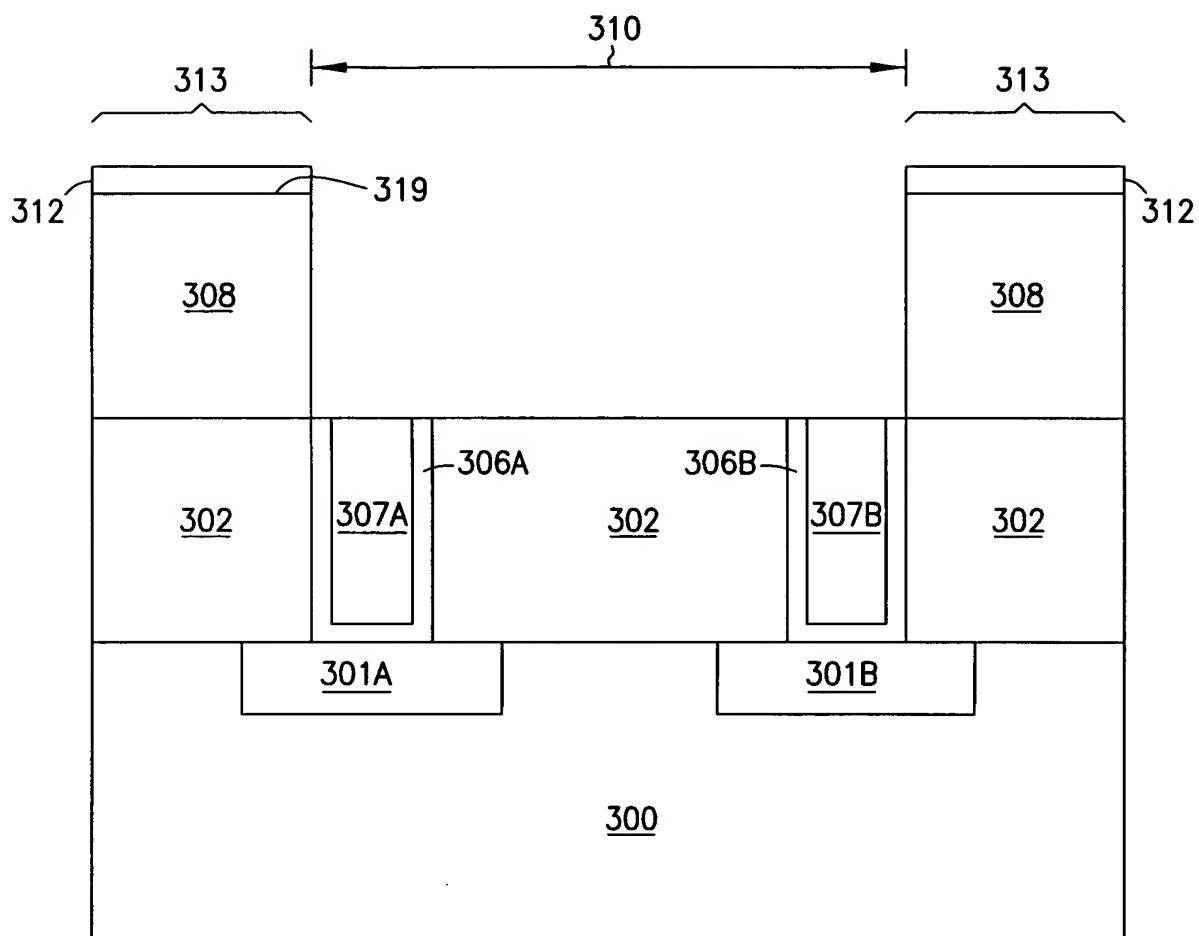


FIG. 3B

TITLE: INTEGRATED CIRCUIT AND SEED LAYERS

INVENTORS NAME: Paul A. Farrar

DOCKET NO.: 303.673US3

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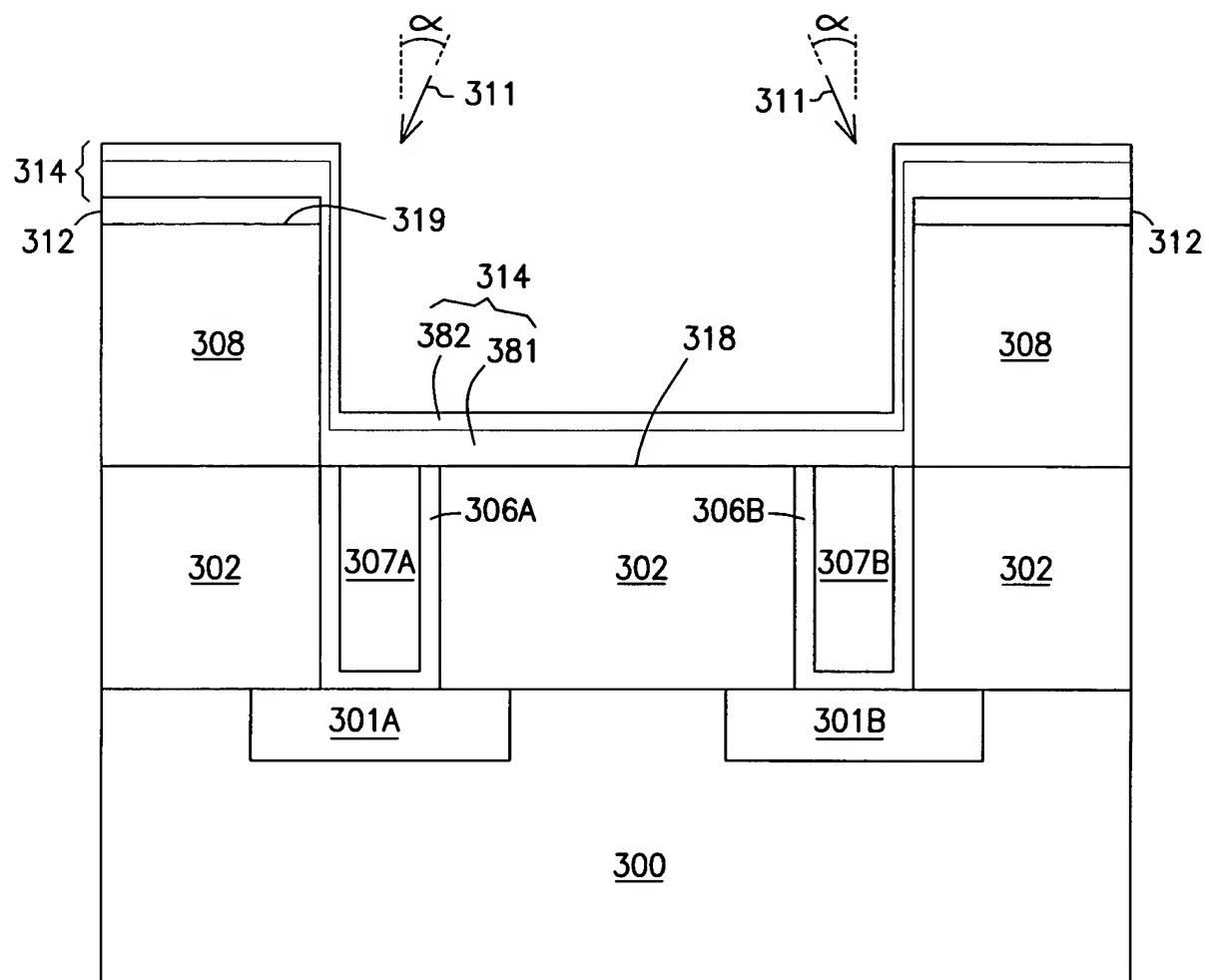


FIG. 3C

TITLE: INTEGRATED CIRCUIT AND SEED LAYERS

INVENTORS NAME: Paul A. Farrar

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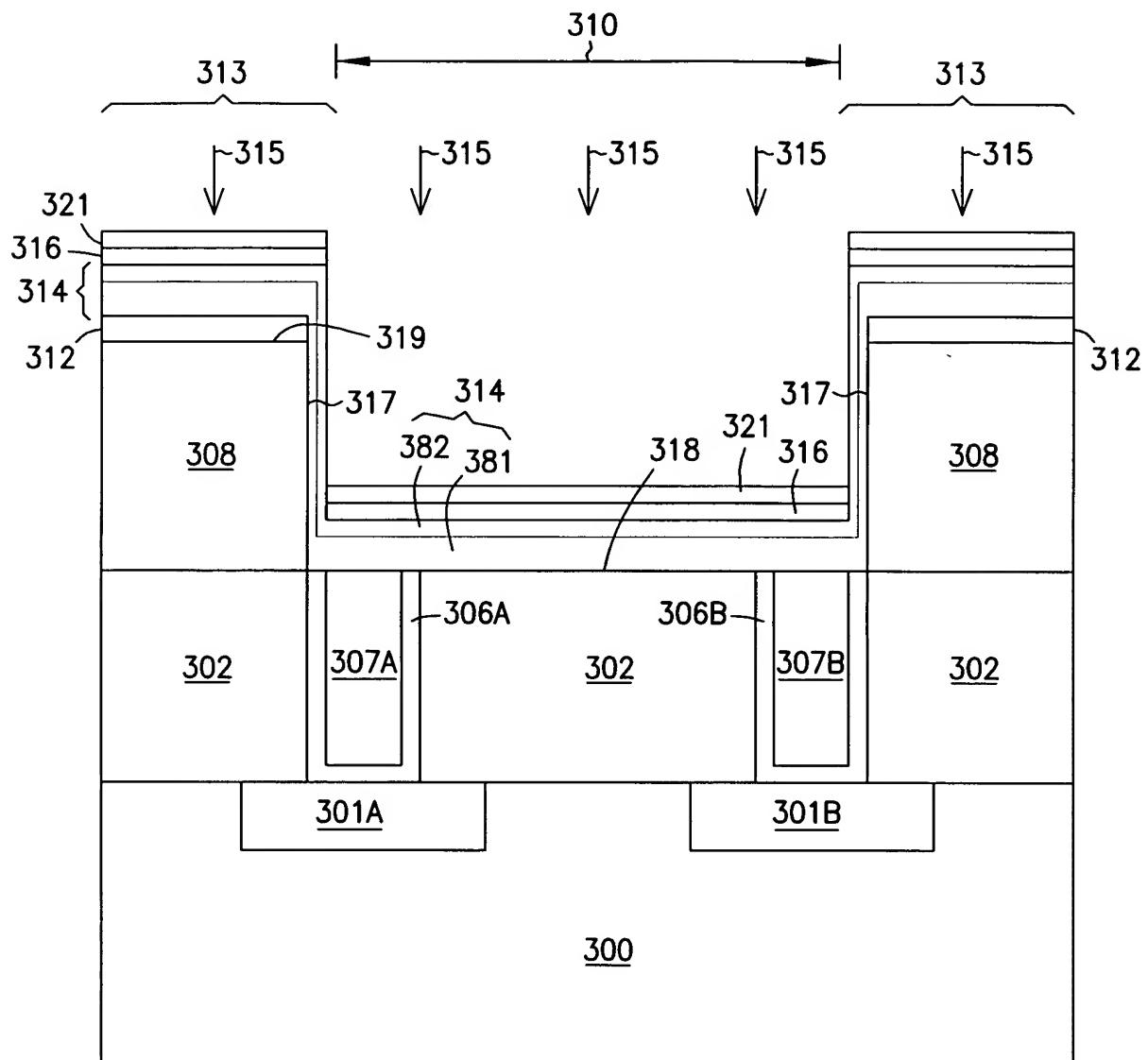


FIG. 3D

TITLE: INTEGRATED CIRCUIT AND SEED LAYERS

INVENTORS NAME: Paul A. Farrar

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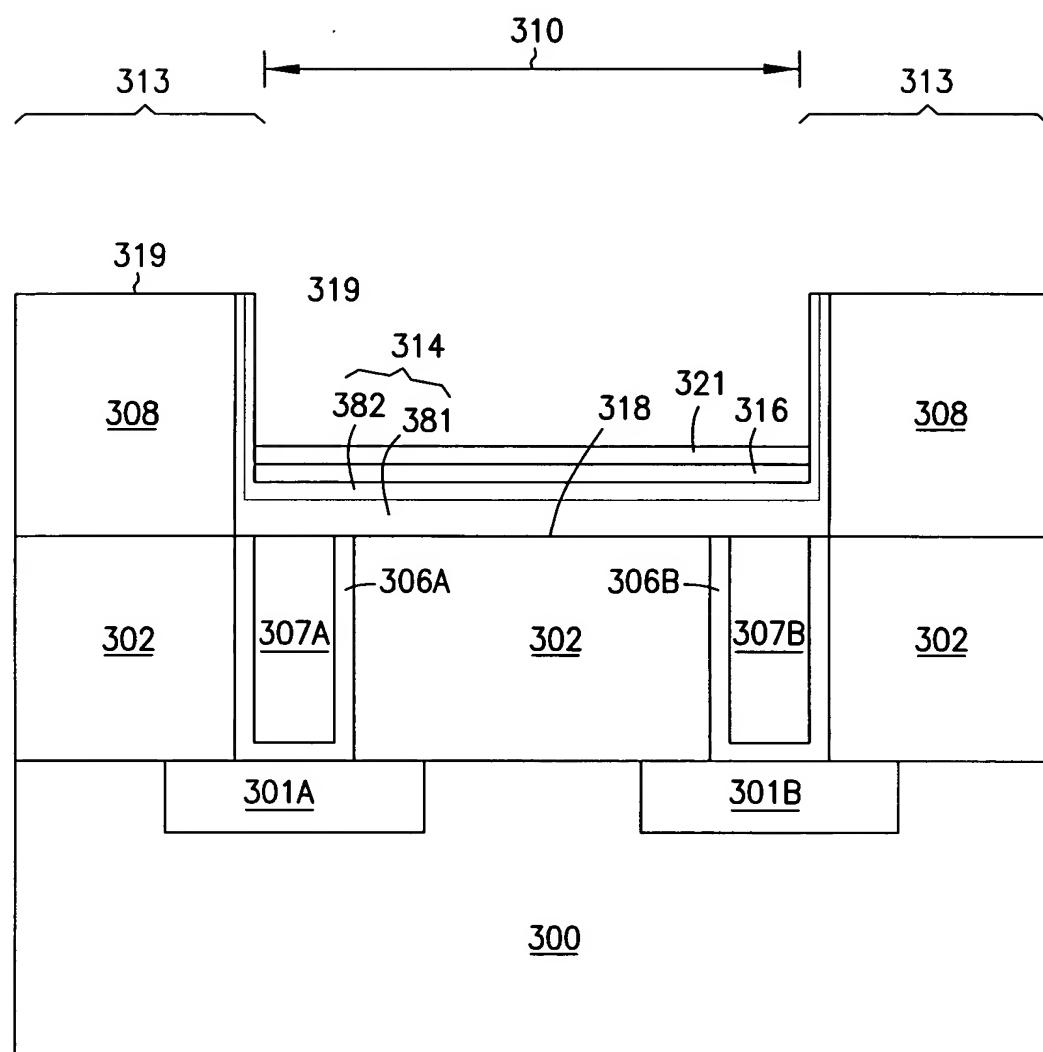


FIG. 3E

TITLE: INTEGRATED CIRCUIT AND SEED LAYERS

INVENTORS NAME: Paul A. Farrar

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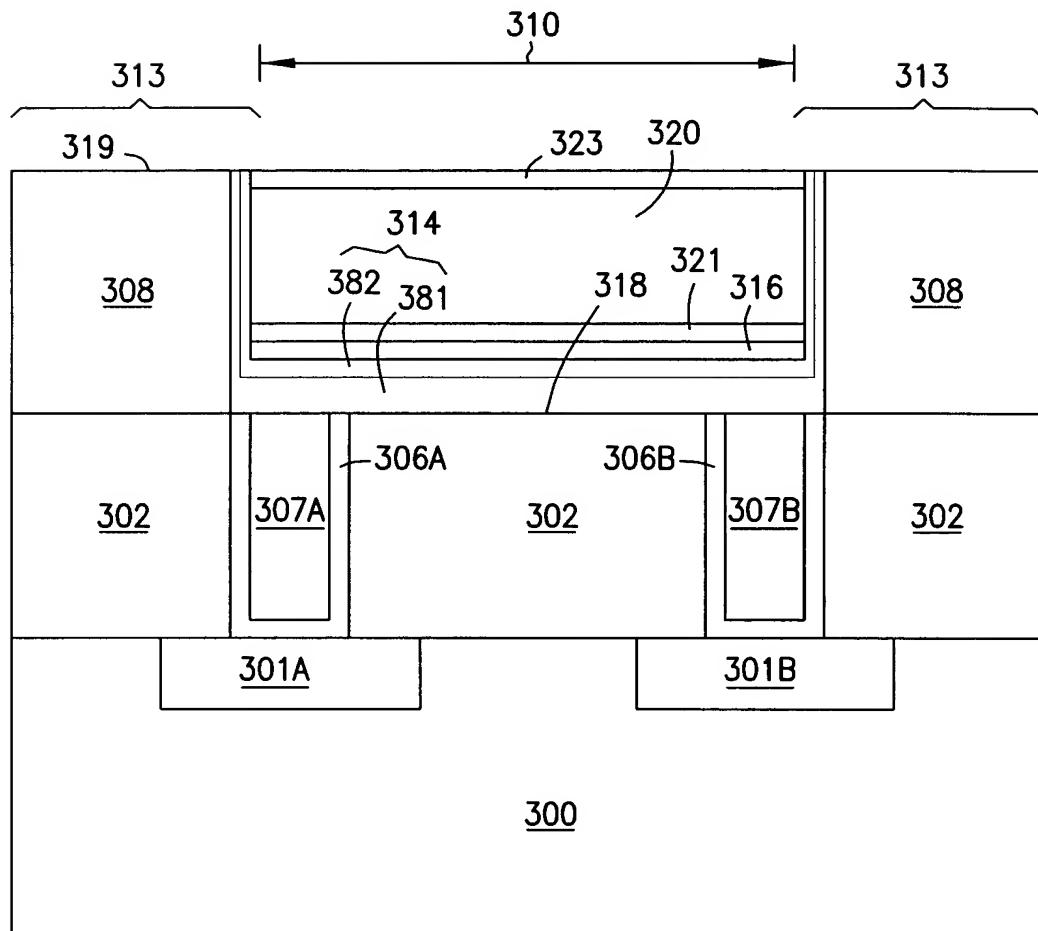


FIG. 3F

TITLE: INTEGRATED CIRCUIT AND SEED LAYERS

INVENTORS NAME: Paul A. Farrar

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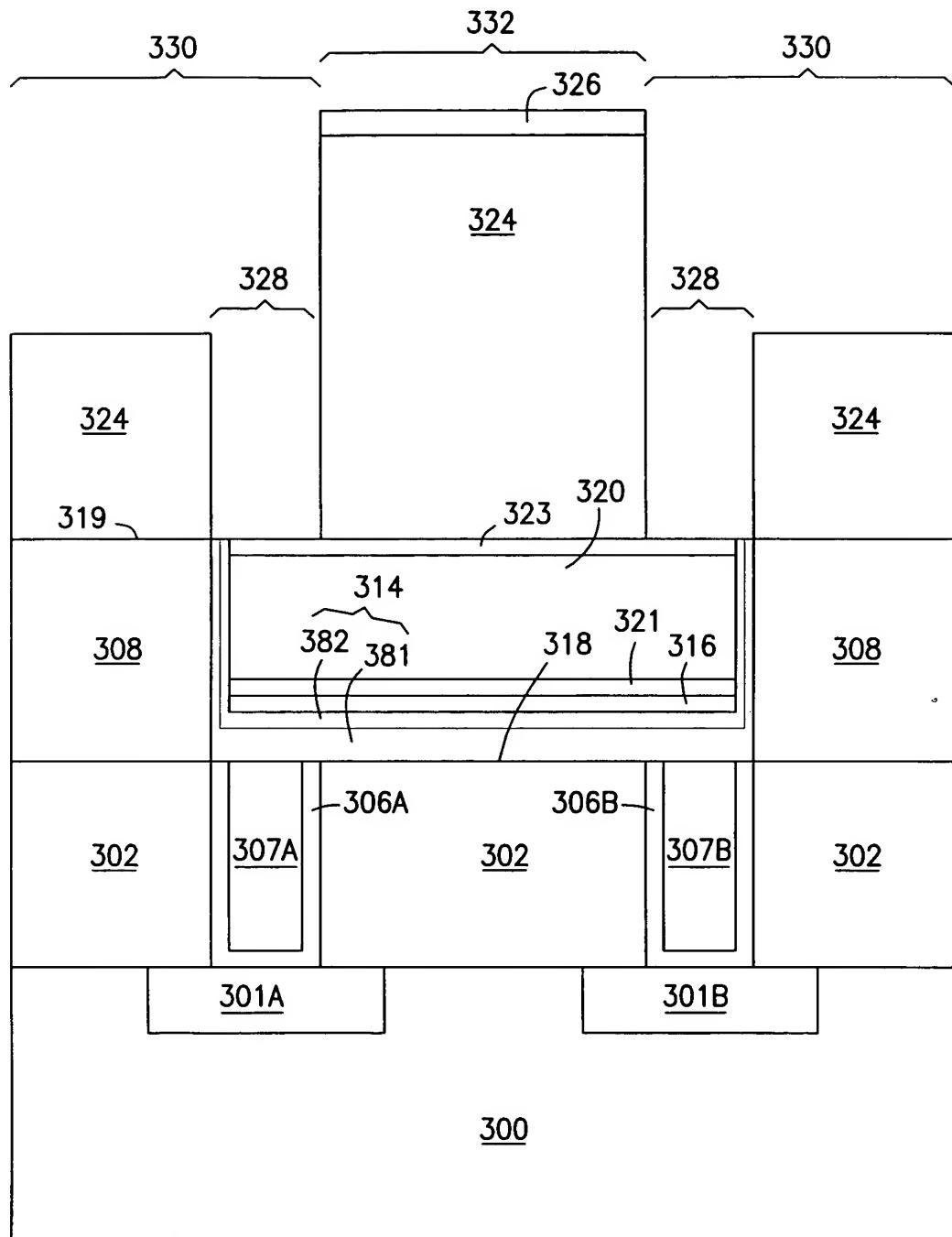


FIG. 3G

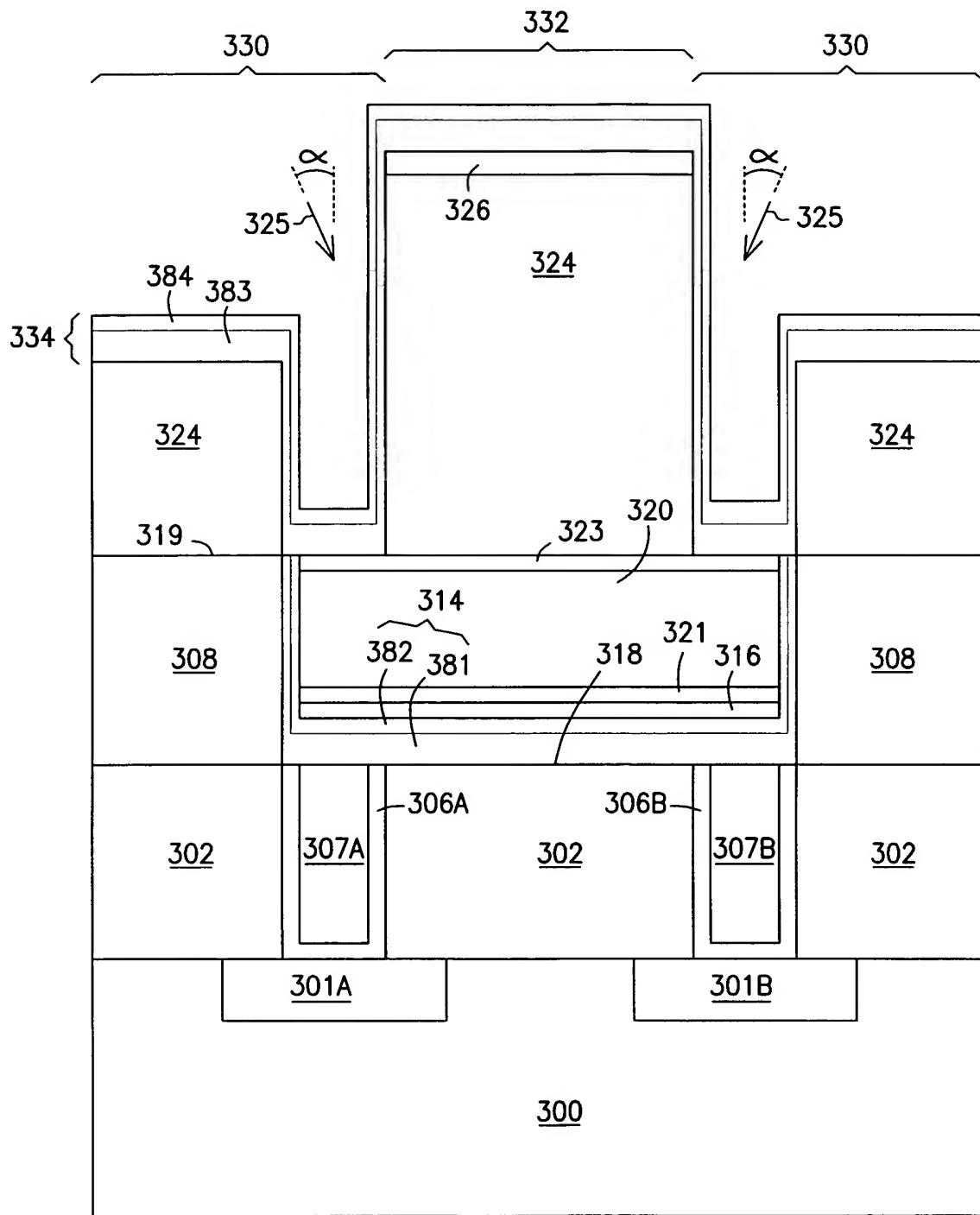


FIG. 3H

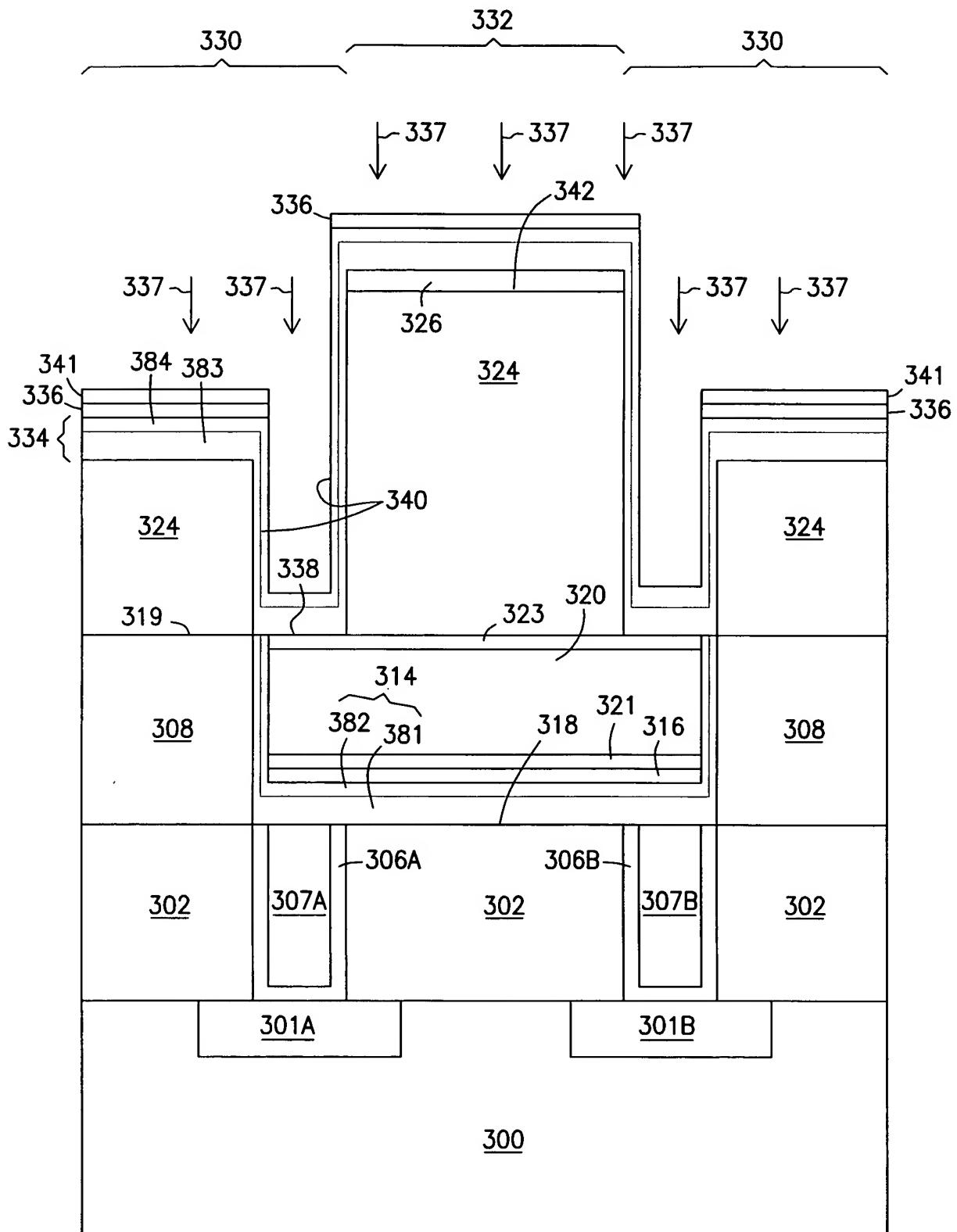


FIG. 31

TITLE: INTEGRATED CIRCUIT AND SEED LAYERS

INVENTORS NAME: Paul A. Farrar

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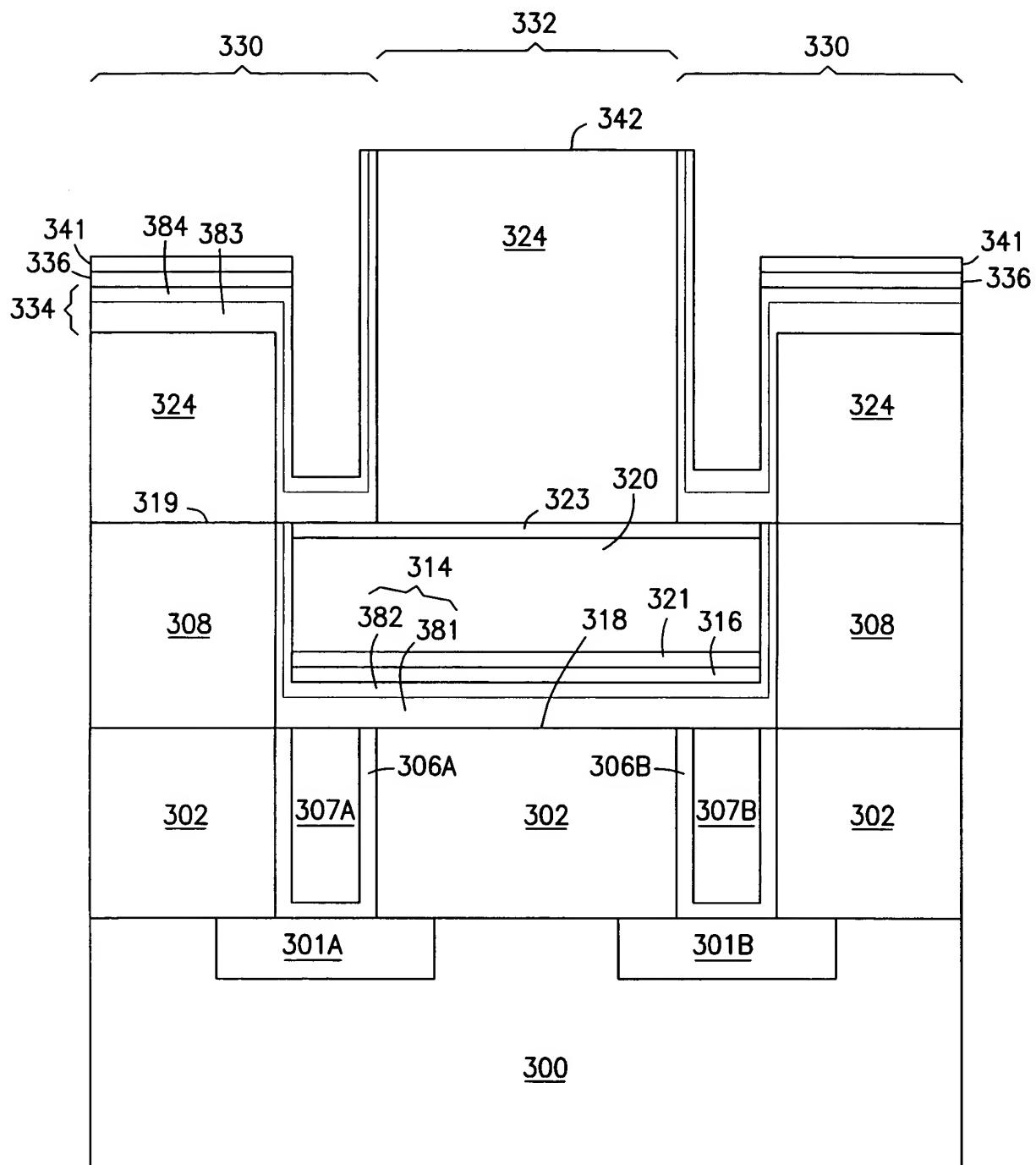


FIG. 3J

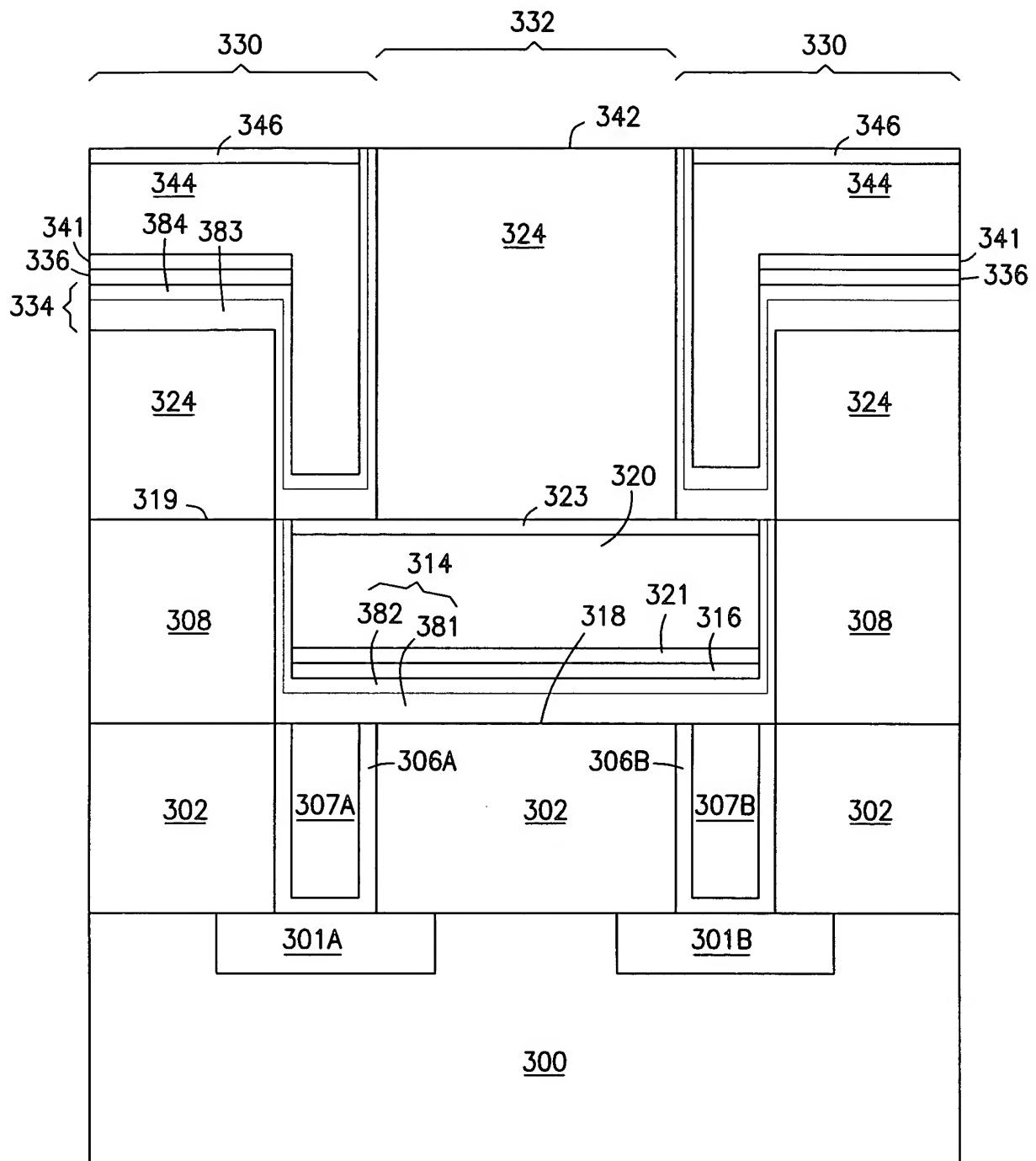


FIG. 3K

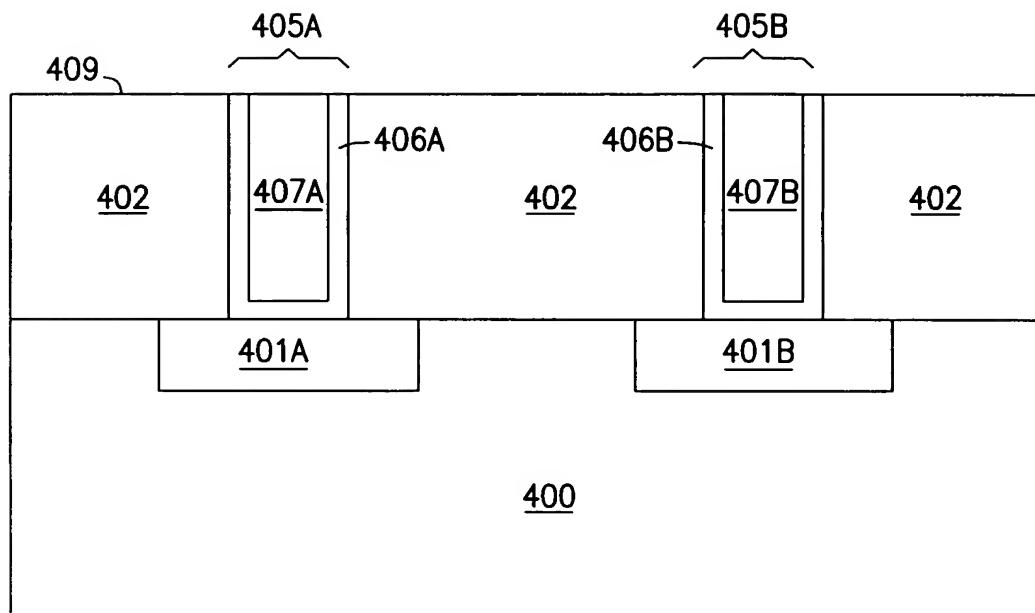


FIG. 4A

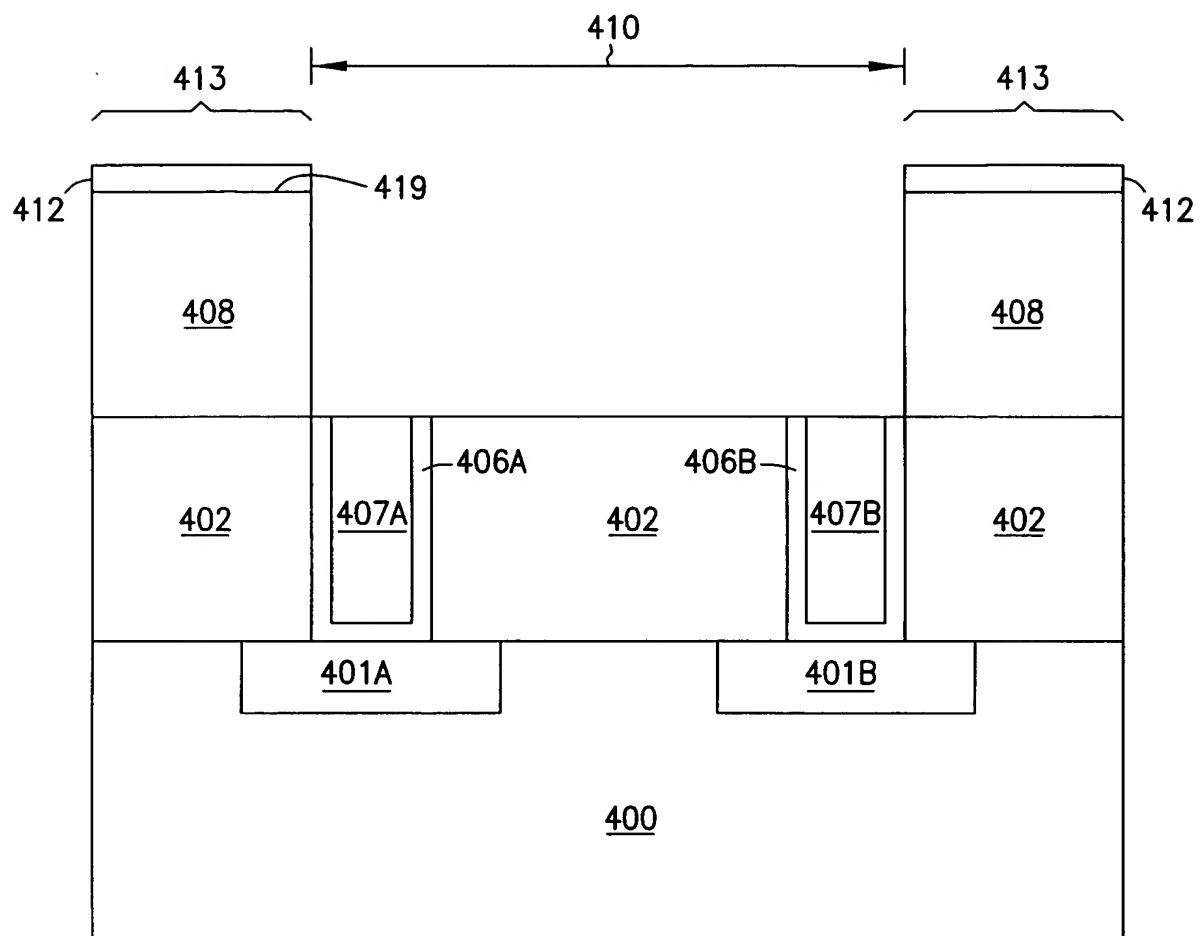


FIG. 4B

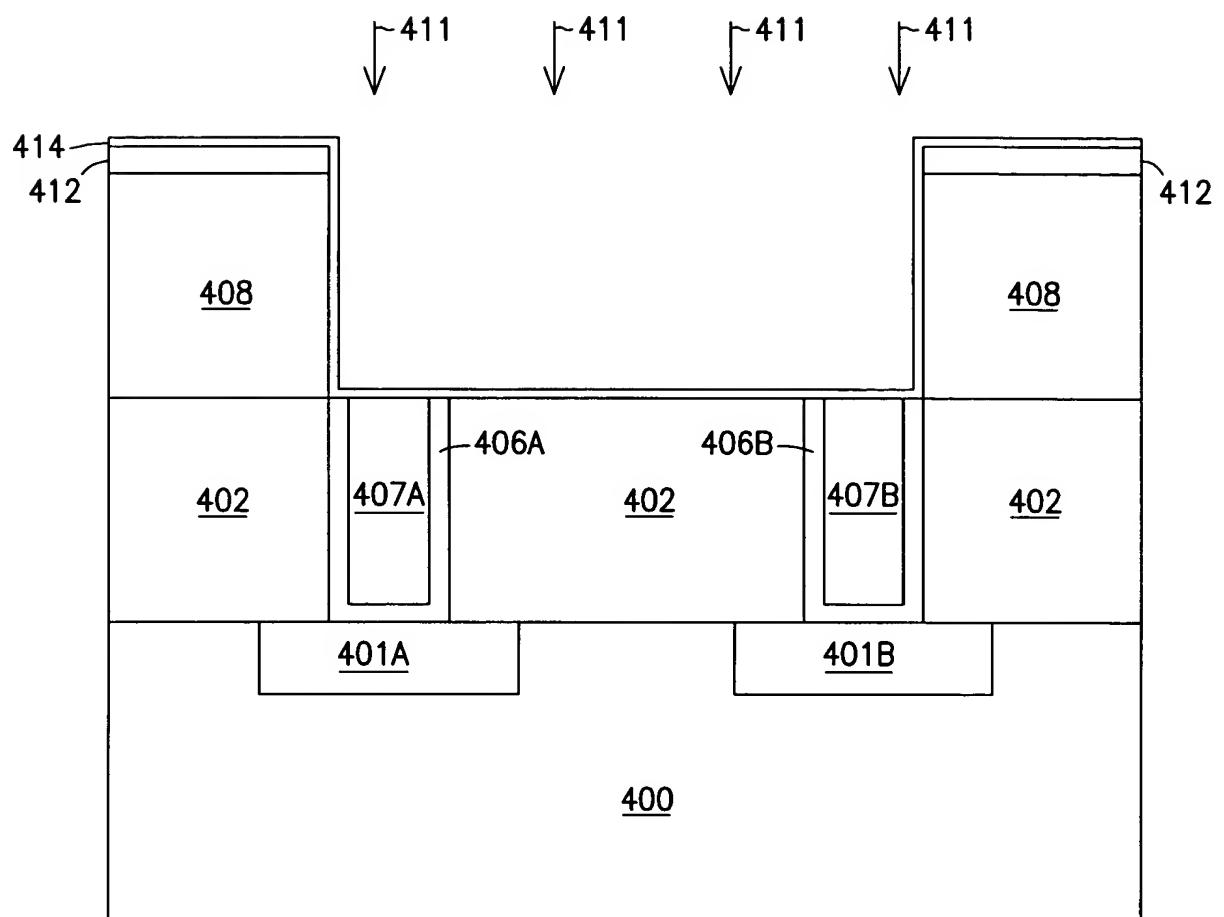


FIG. 4C

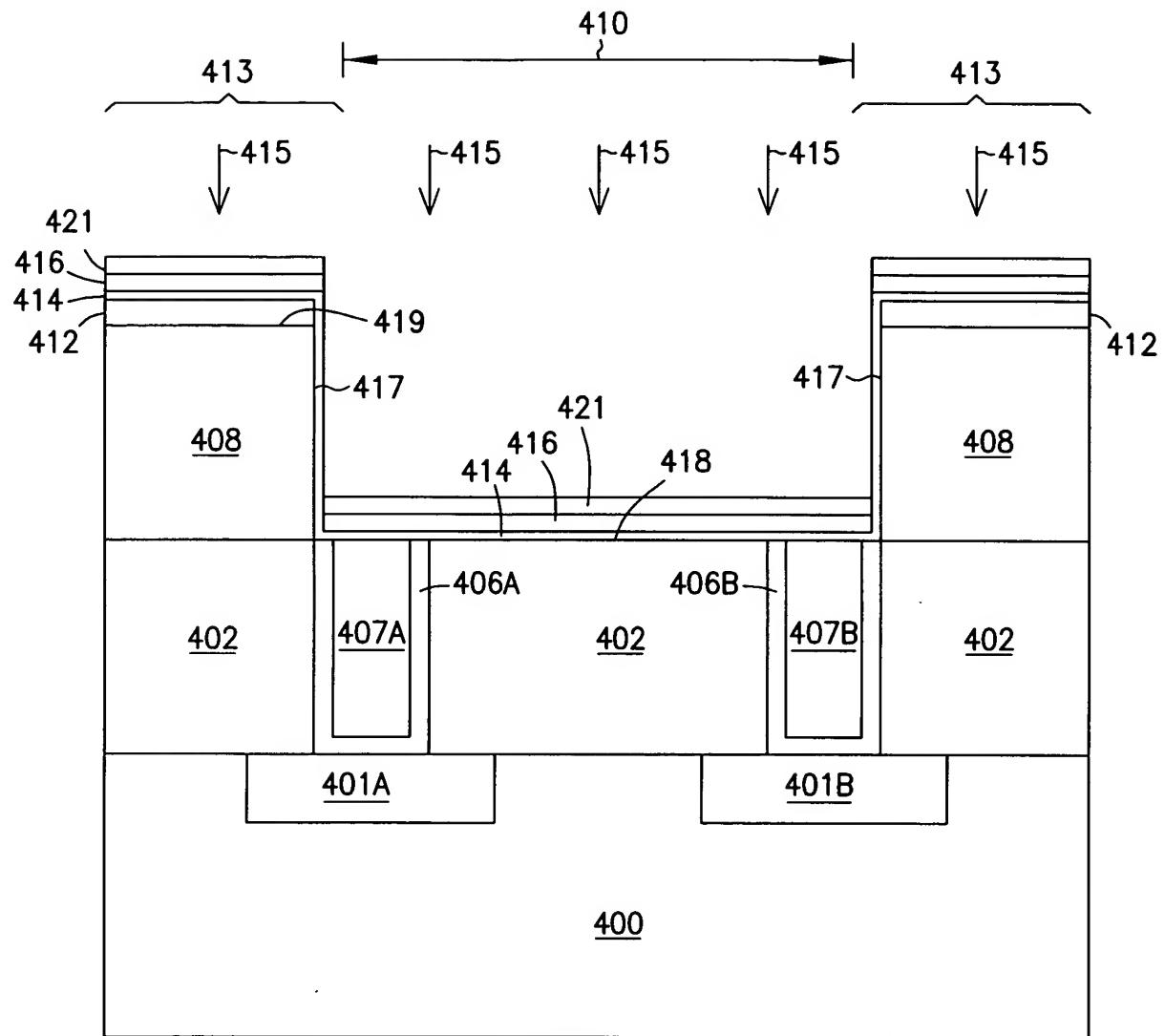


FIG. 4D

TITLE: INTEGRATED CIRCUIT AND SEED LAYERS

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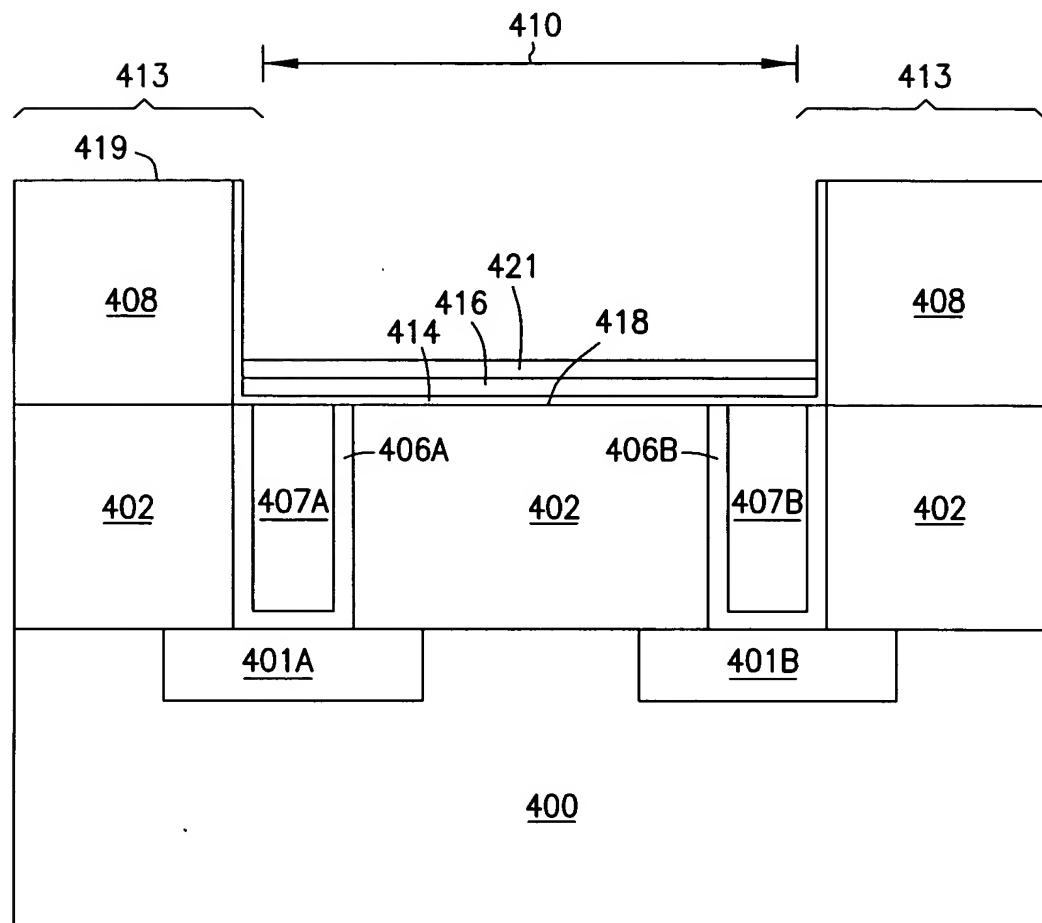


FIG. 4E

TITLE: INTEGRATED CIRCUIT AND SEED LAYERS
INVENTORS NAME: Paul A. Farrar
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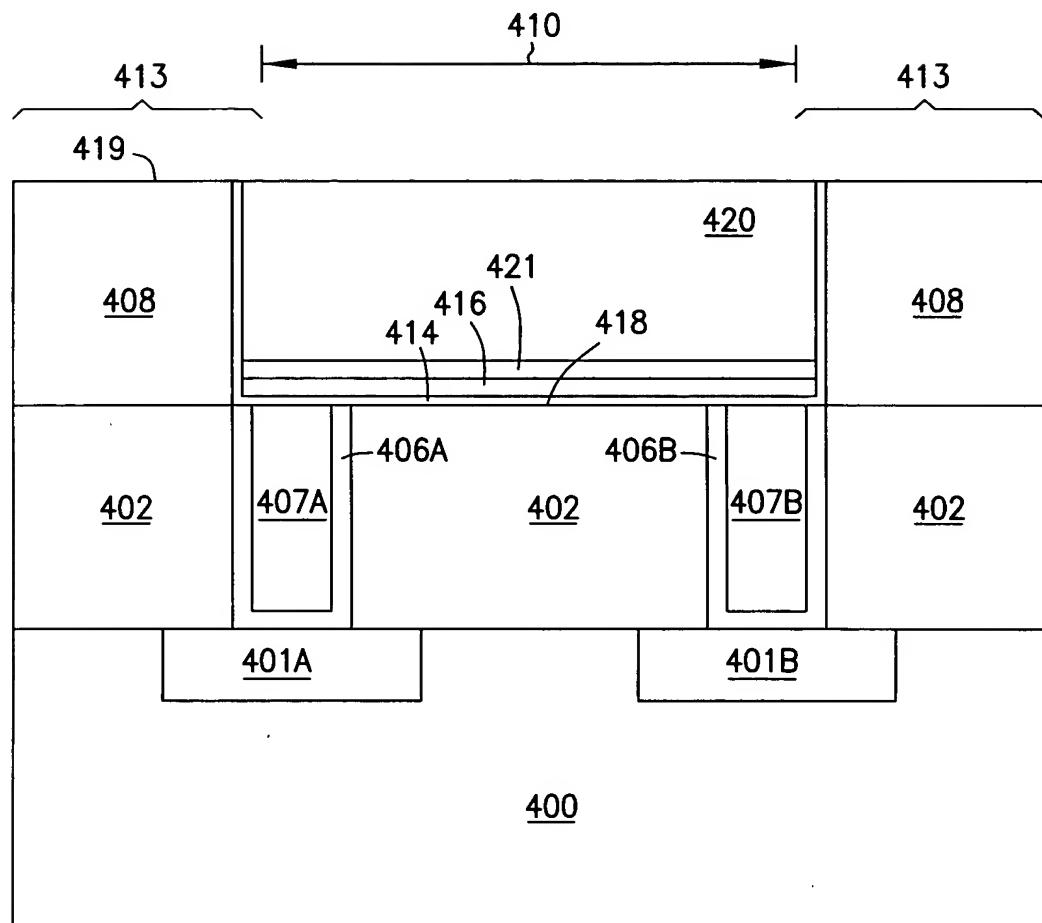


FIG. 4F

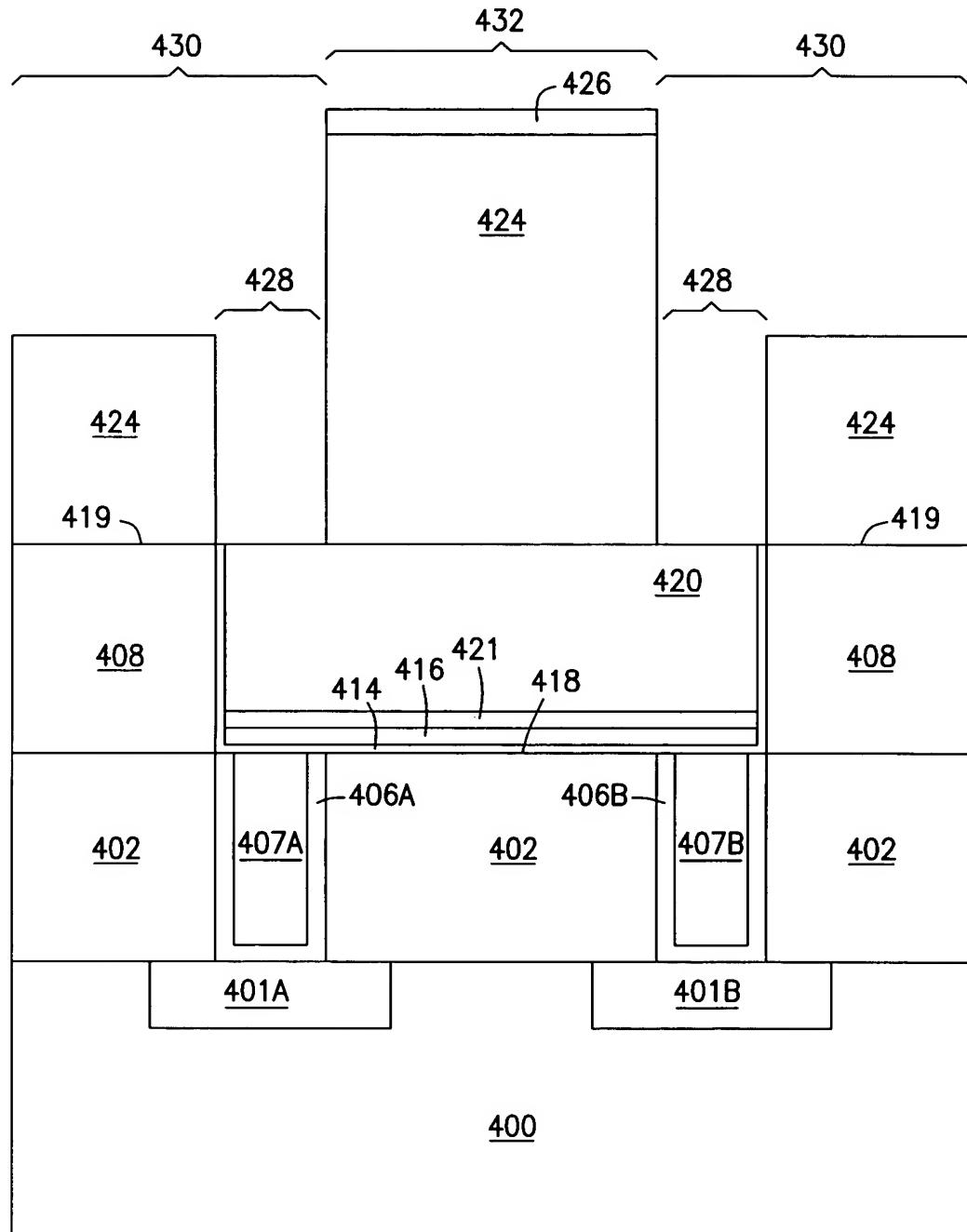


FIG. 4G

TITLE: INTEGRATED CIRCUIT AND SEED LAYERS

INVENTORS NAME: Paul A. Farrar

DOCKET NO.: 303.673US3

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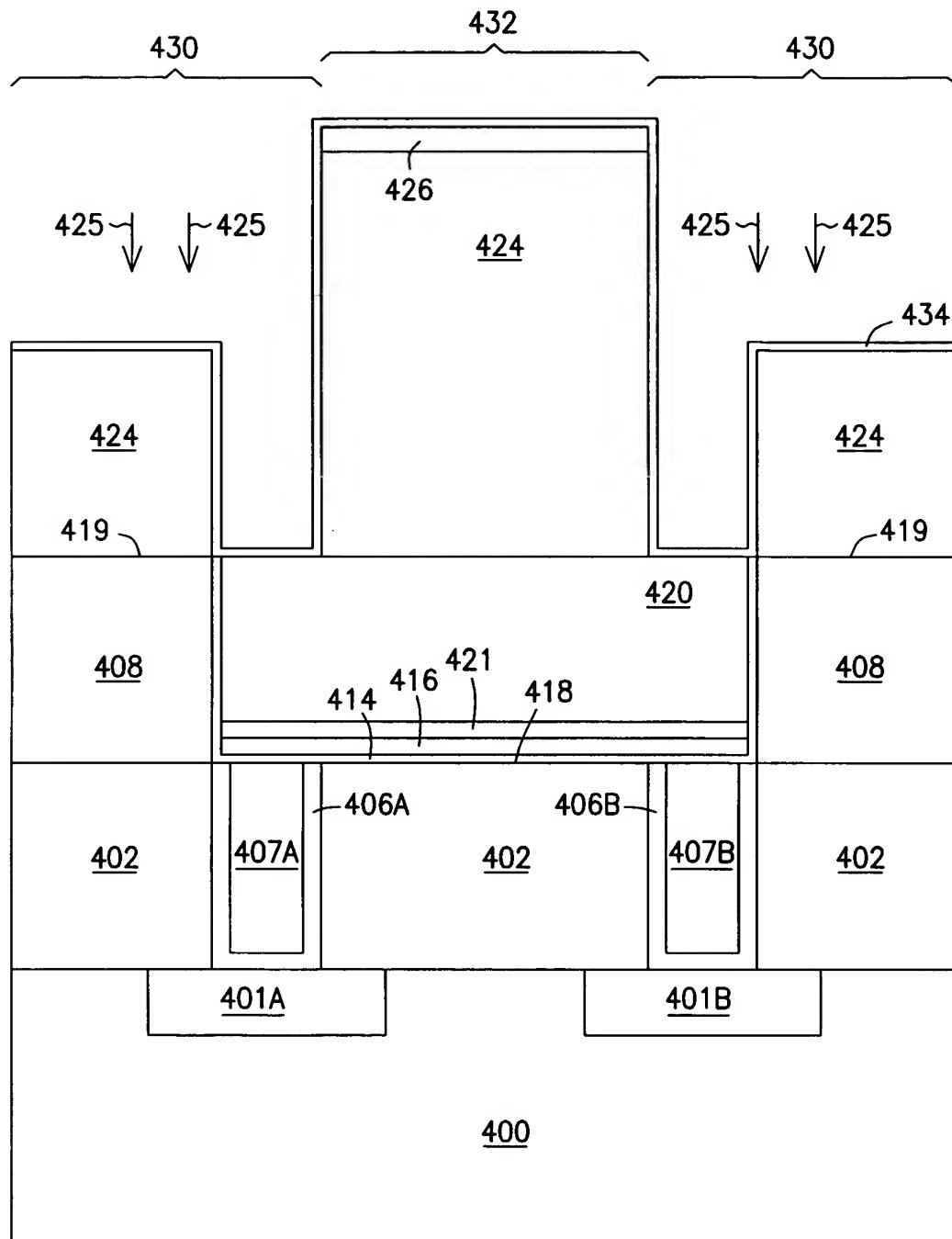


FIG. 4H

TITLE: INTEGRATED CIRCUIT AND SEED LAYERS
INVENTORS NAME: Paul A. Farrar
DOCKET NO.: 303.673US3

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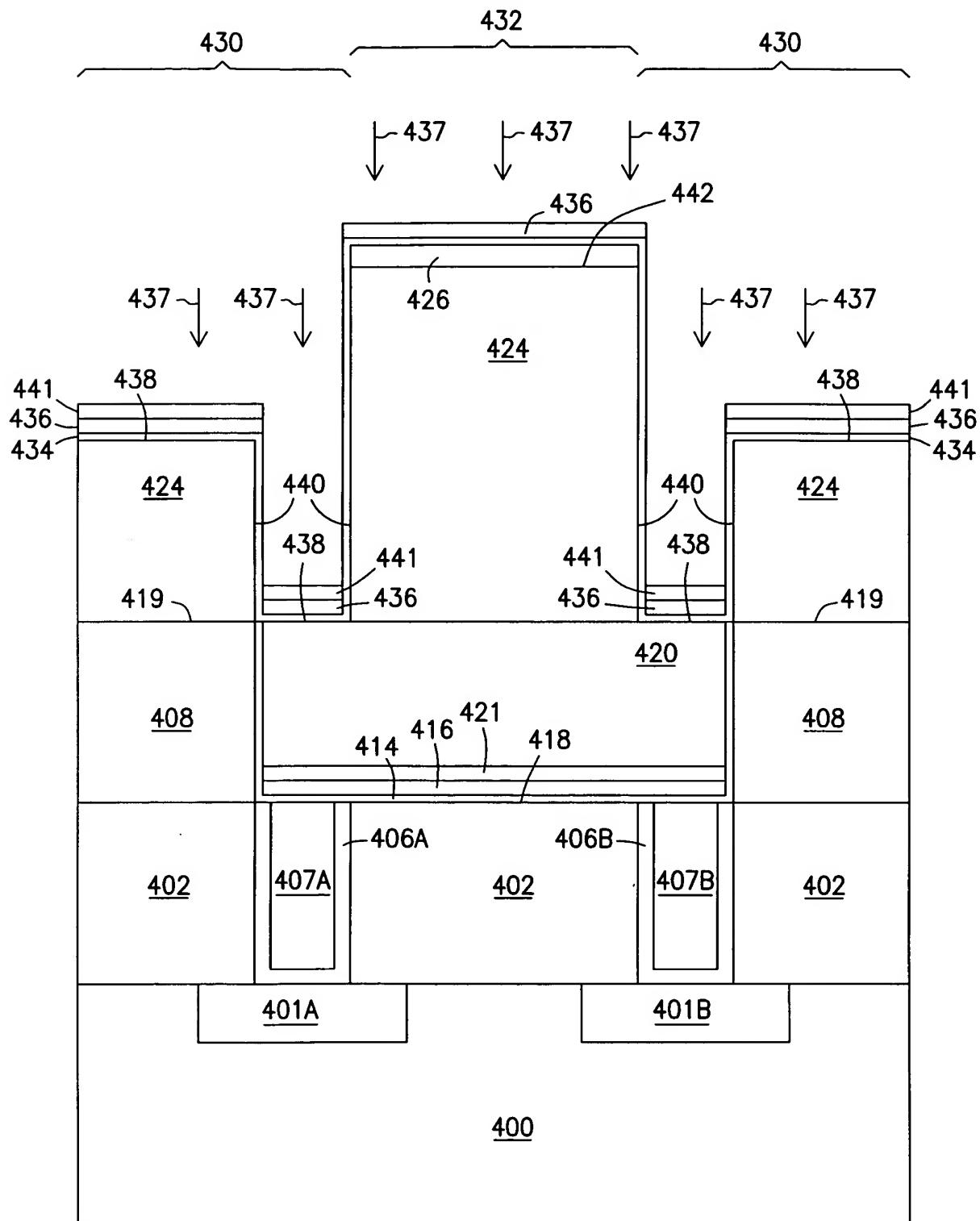


FIG. 4I

TITLE: INTEGRATED CIRCUIT AND SEED LAYERS
INVENTORS NAME: Paul A. Farrar
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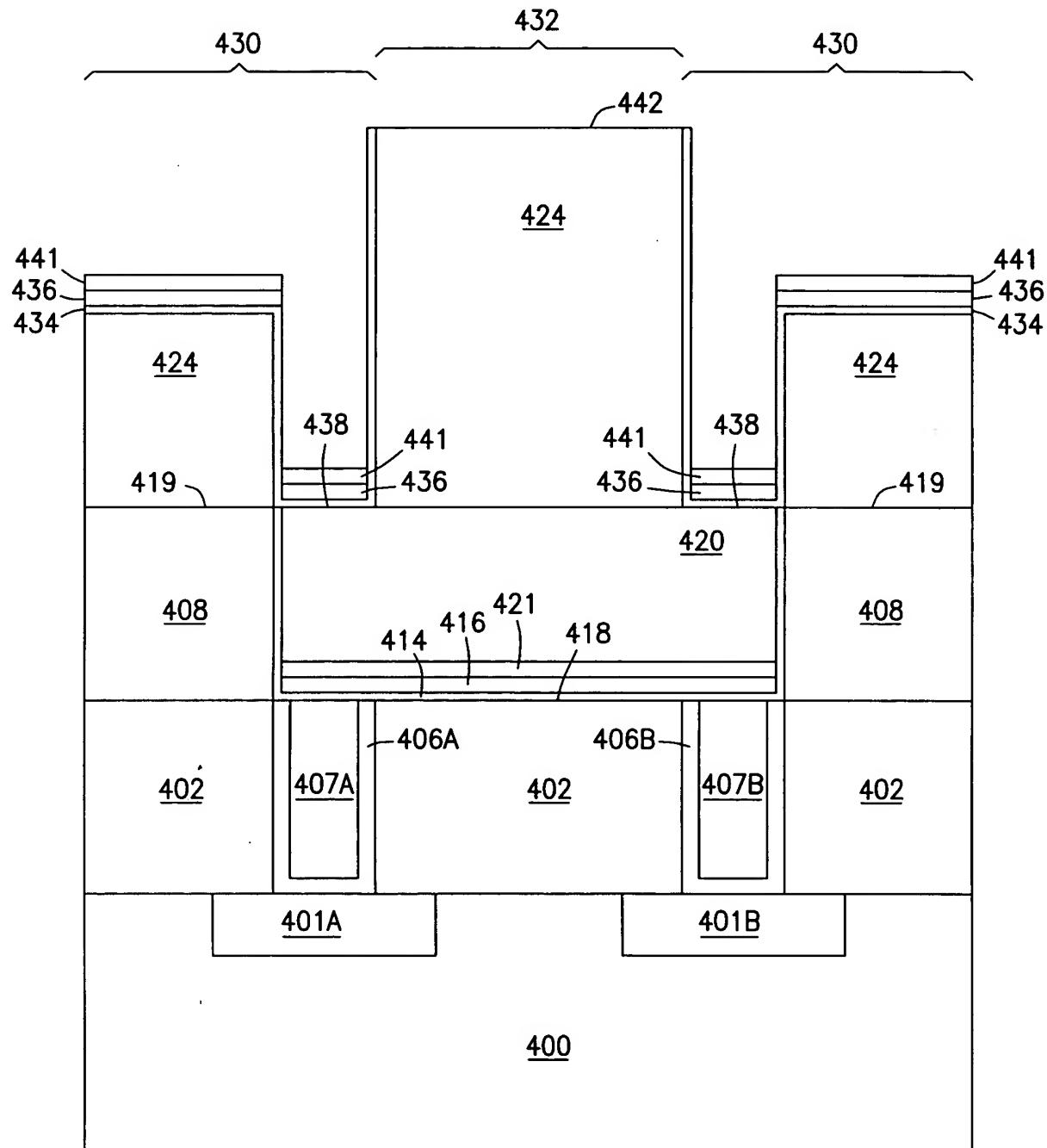


FIG. 4J

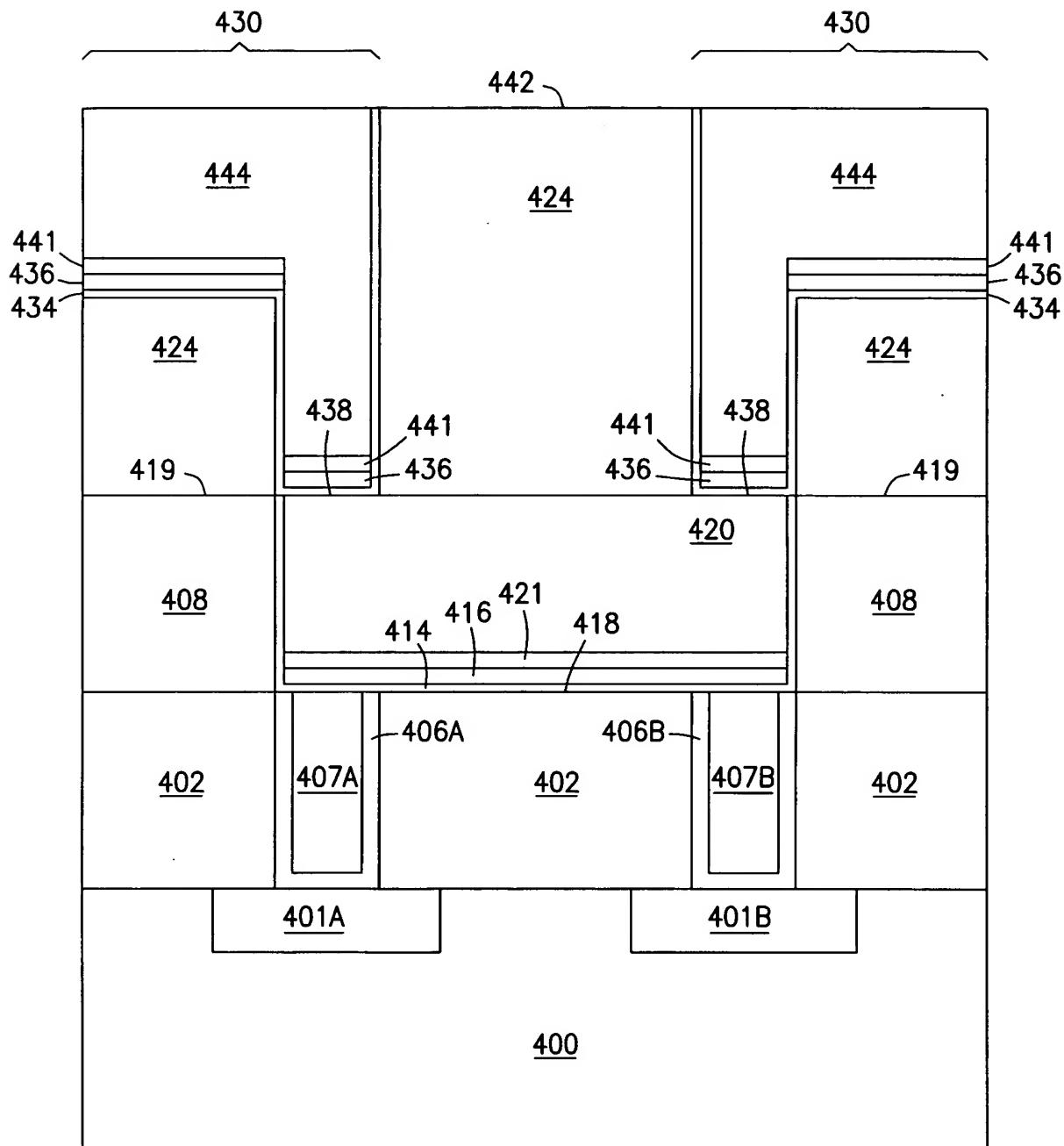


FIG. 4K

TITLE: INTEGRATED CIRCUIT AND SEED LAYERS
INVENTORS NAME: Paul A. Farrar
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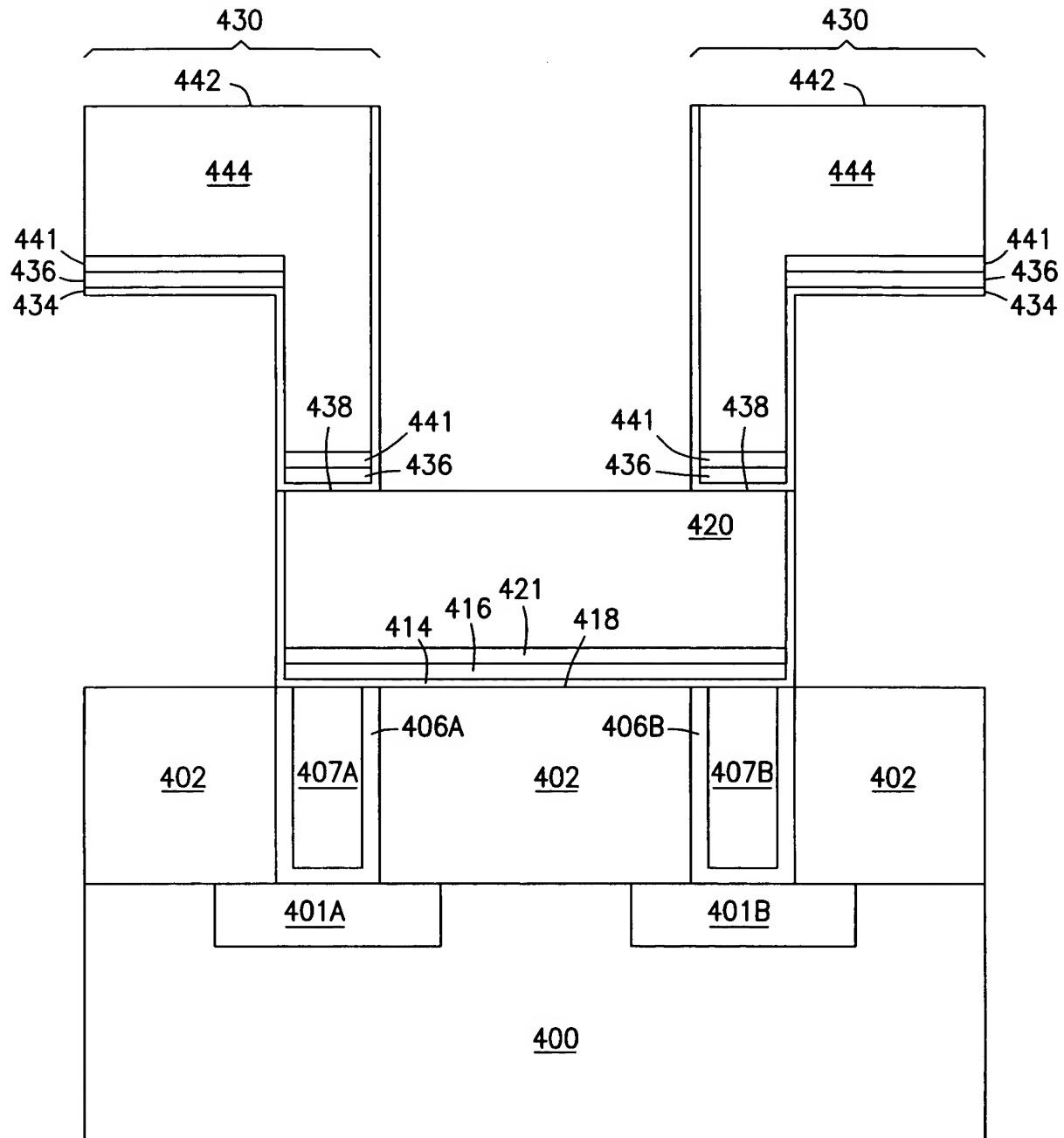


FIG. 4L

TITLE: INTEGRATED CIRCUIT AND SEED LAYERS

INVENTORS NAME: Paul A. Farrar

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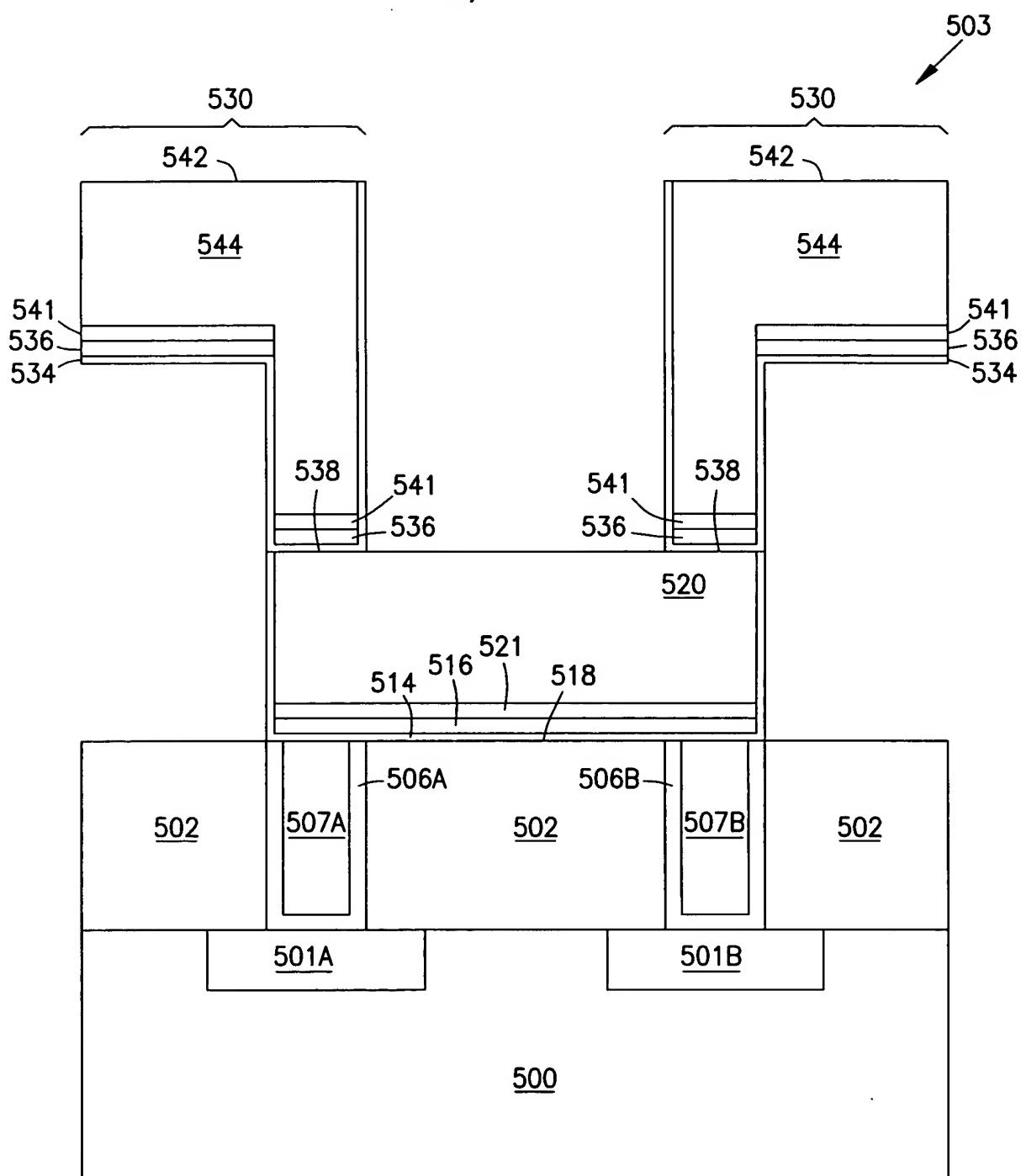


FIG. 5

TITLE: INTEGRATED CIRCUIT AND SEED LAYERS
INVENTORS NAME: Paul A. Farrar
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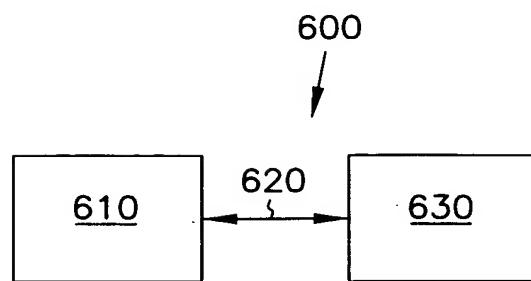


FIG. 6